

FIG. 1

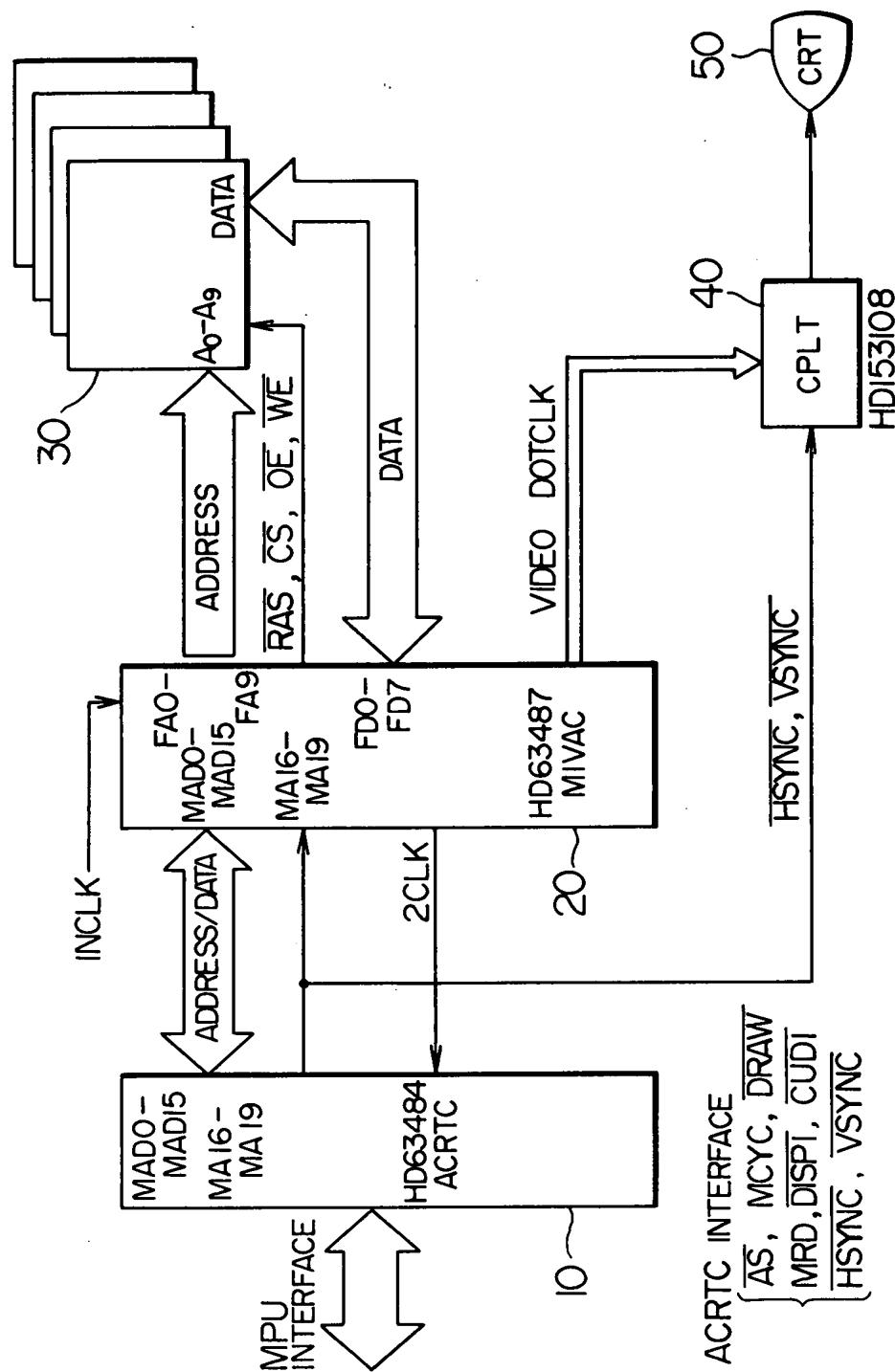


FIG. 2

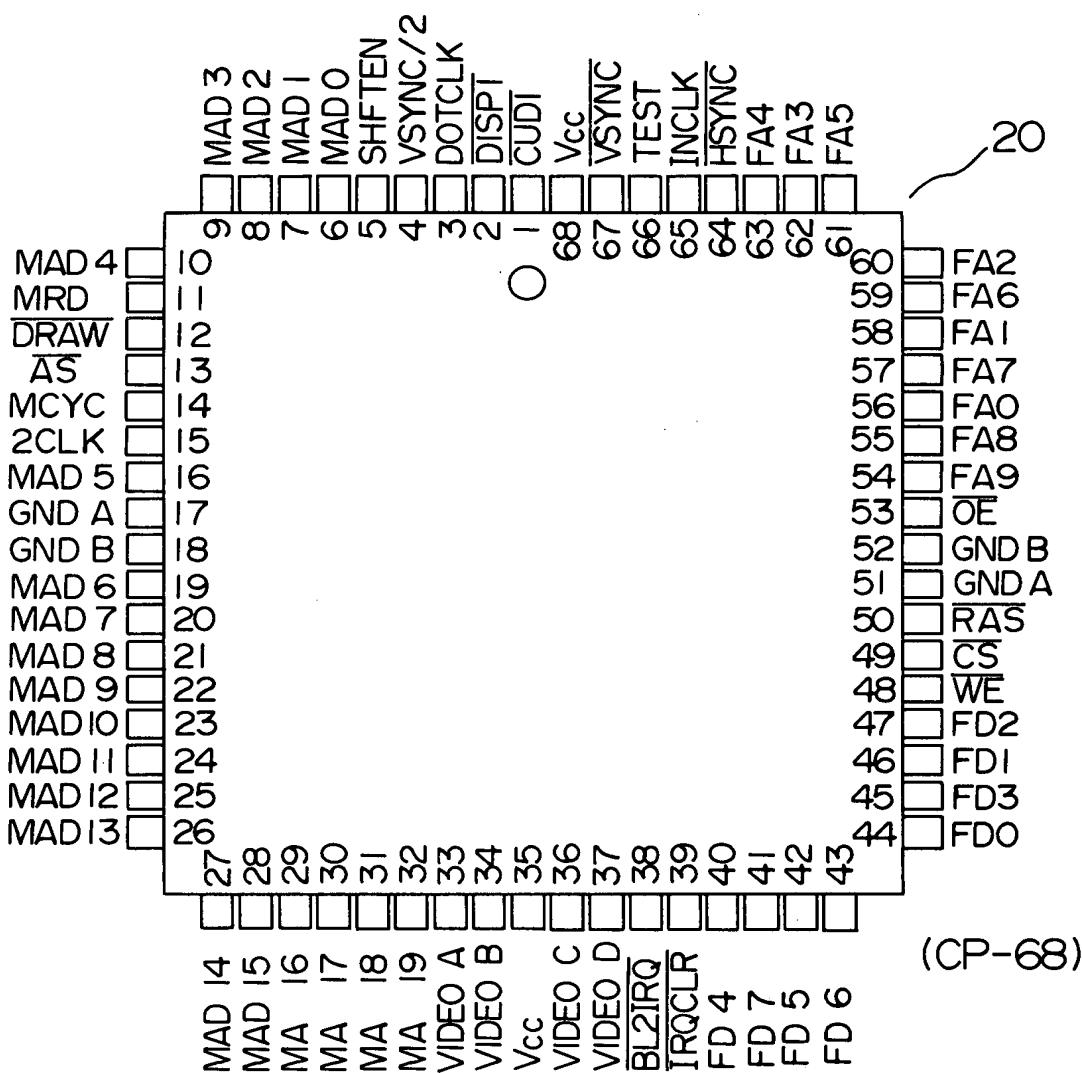


FIG. 3a

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+ 5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPLIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC, NAMELY, HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. MCYC INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	DRAW	INPUT	DRAW SIGNAL FROM ACRTC IS INPUTTED. DRAW INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. DRAW IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	AS	INPUT	AS SIGNAL IS INPUTTED FROM ACRTC AS INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	Hsync	INPUT	Hsync SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF HSYNC="LOW" AND DRAW="HIGH", IF AS PULSE IS RECEIVED, CS BEFORE RAS REFRESH OPERATION IS CARRIED OUT.
	67	Vsync	INPUT	Vsync SIGNAL IS INPUTTED FROM ACRTC. RECEIVED Vsync IS DIVIDED BY TWO SO AS TO OUTPUTTED AS Vsync/2 SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	Disp 1	INPUT	Disp 1 SIGNAL IS INPUTTED FROM ACRTC. Disp 1 INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	CUD 1	INPUT	CUD 1 SIGNAL IS INPUTTED FROM ACRTC. CUD 1 IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6-10 16 19-28	MADO -MAD15	INPUT/OUTPUT	MODO-MAD15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC="LOW", AS DATA INPUT/OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC="HIGH".
29-32	MA16- MA19	INPUT		FRAME BUFFER ACCESS ADDRESS MA16-MA19 IS INPUTTED FROM ACRTC.

F I G. 3b

ITEM	TERMI-NAL NO.	TERMI-NAL NAME	INPUT/OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	RAS	OUTPUT	RAS TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	CS	OUTPUT	CS TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	WE	OUTPUT	WE TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	OE	OUTPUT	OE TIMING SIGNAL IS OUTPUTTED FOR DRAM.
CRT DISPLAY INTERFACE SIGNAL	56,58 60,62 63,61 59,57 55,54	FA0 - FA 9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF 0 - VCF 3 AND VMD 0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FDO - FD7	INPUT/OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD 0 - FD3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD 0 - FD7 ARE USED.
	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 OR 4. DIVISION RATIO IS SET DEPENDING ON VCF 0 - VCF 3 OF ATTRIBUTE CODE.
	33,34 36,37	VIDEO A - VIDEO D	OUTPUT	VIDEO A-SIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHFTEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF 0 - VCF 3.
OTHERS	5	SHFTEN	OUTPUT	SHFTEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, DISP1 FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, DISP1 IS ELONGATED BACKWARD BY TWO CYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC/2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. VSYNC IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
	38	BL2IRQ	OUTPUT	BL2IRQ IS SET BY BLINK 2(MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK 2 IS AT "HIGH" LEVEL, BL2IRQ IS SET TO "LOW" LEVEL.
	39	IRQCLR	INPUT	IRQCLR SIGNAL IS USED TO CLEAR BL2IRQ SIGNAL. WHEN "LOW" IS INPUTTED TO IRQCLR, BL2IRQ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

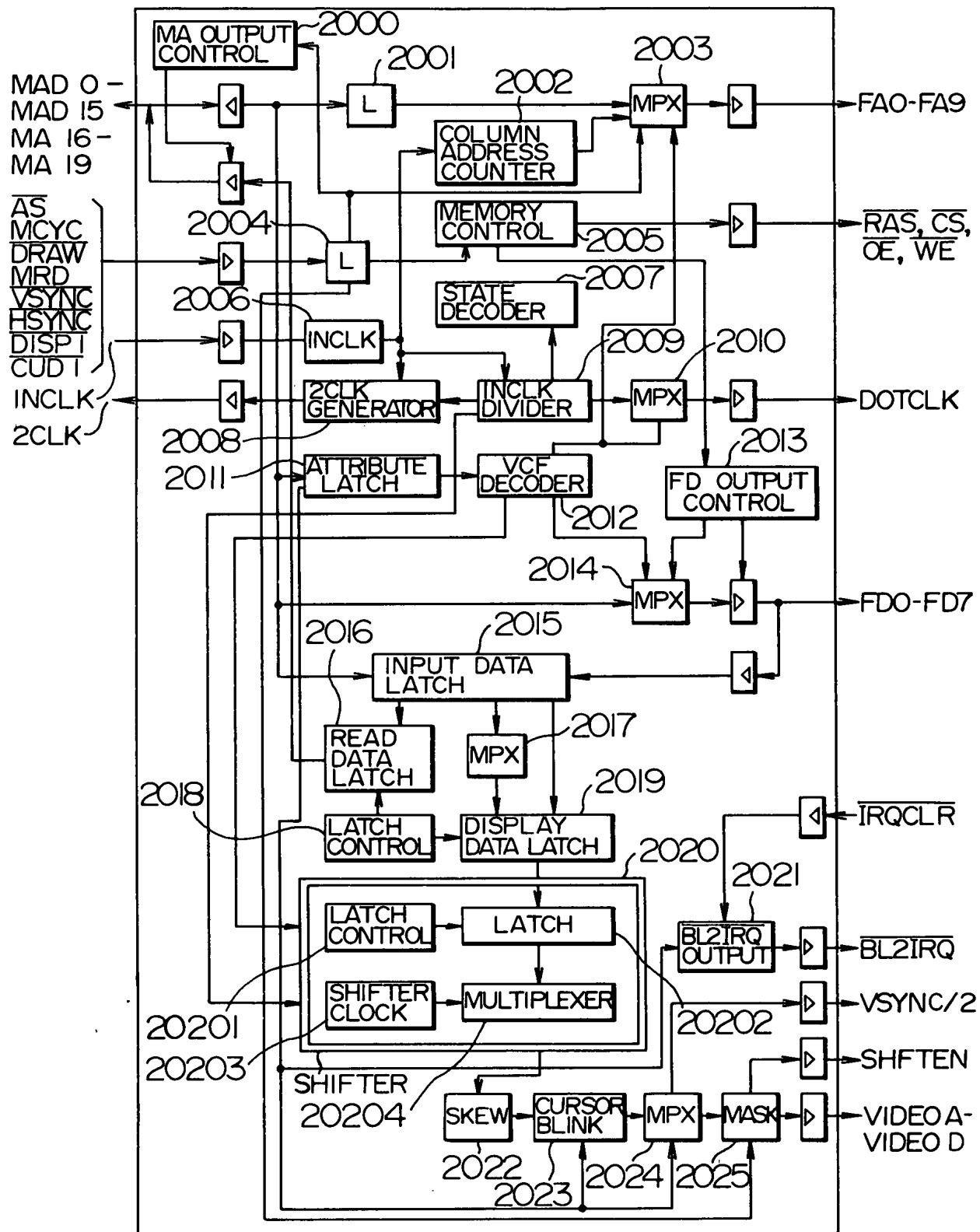


FIG. 5a

1-CHIP MEMORY

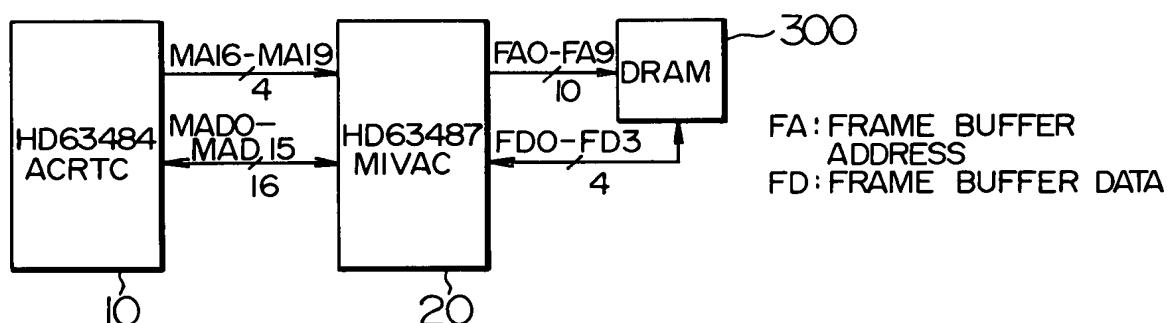


FIG. 5b 2-CHIP MEMORY

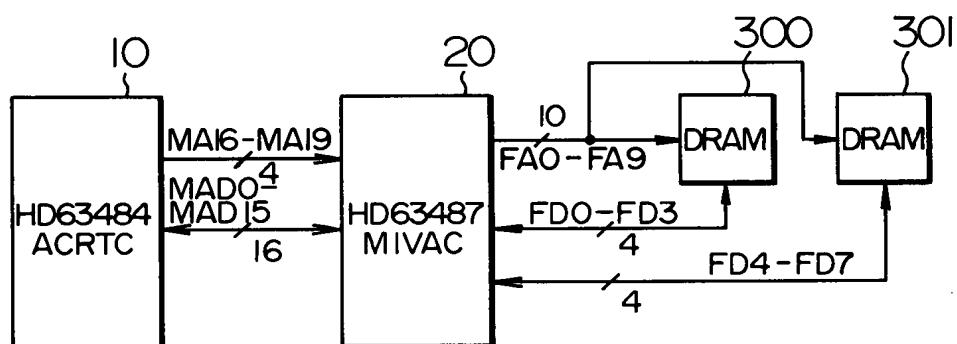


FIG. 5c

4-CHIP MEMORY

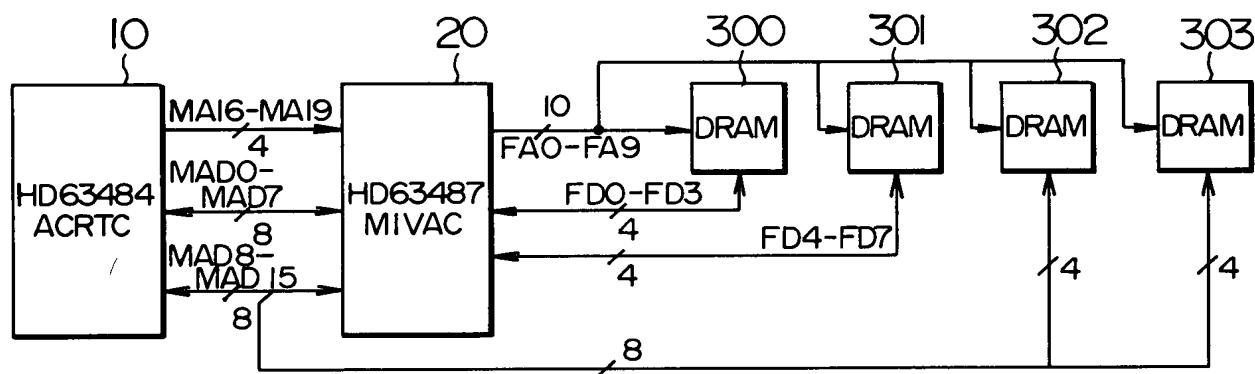


FIG. 6

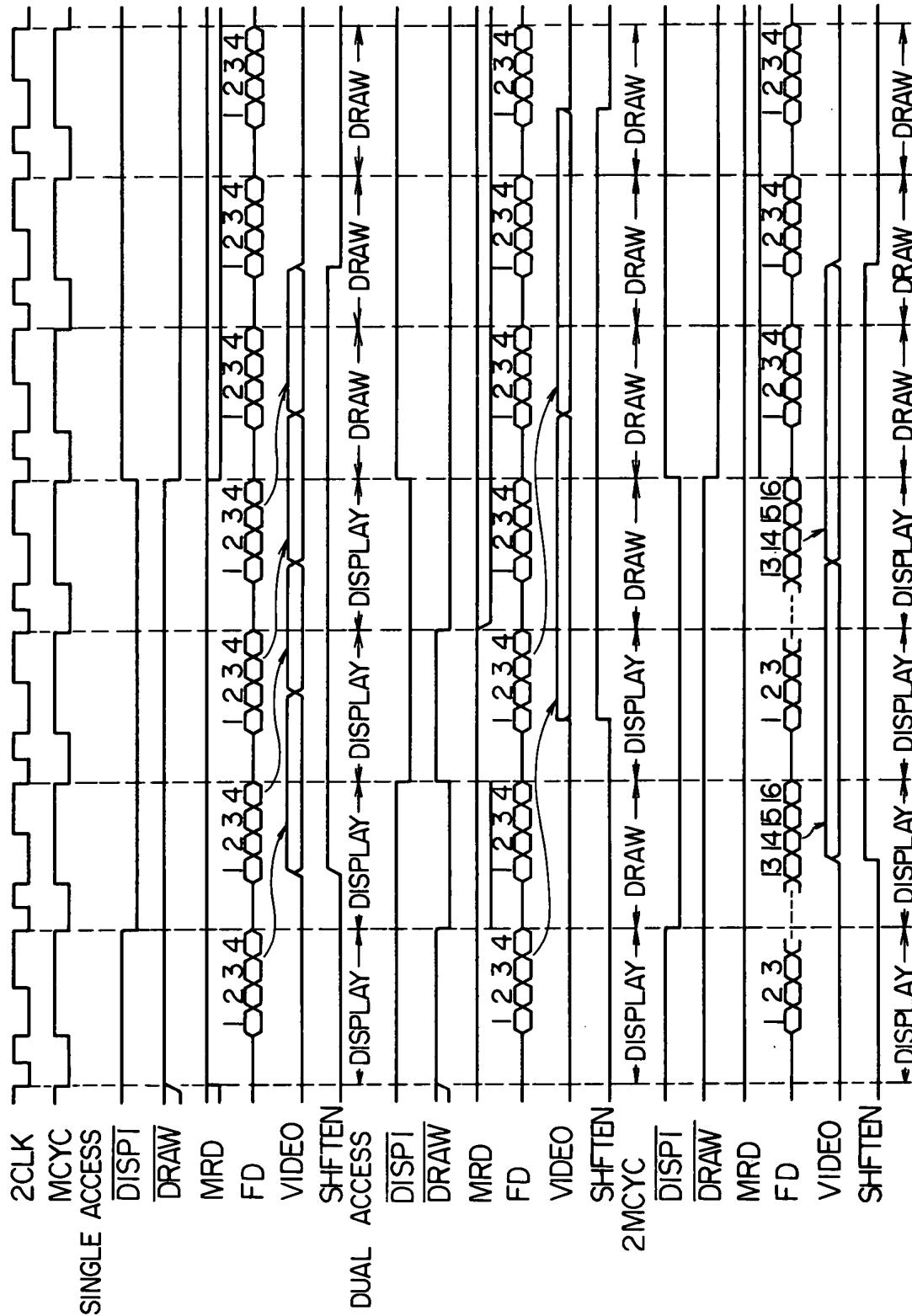


FIG. 7

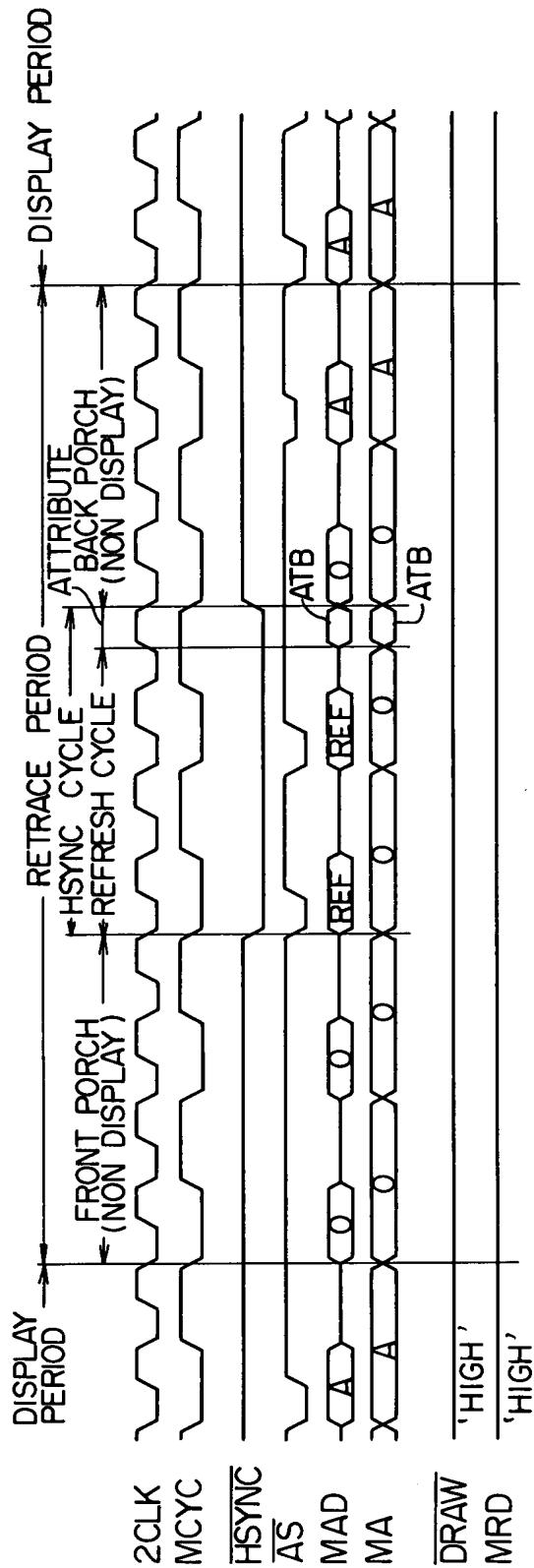
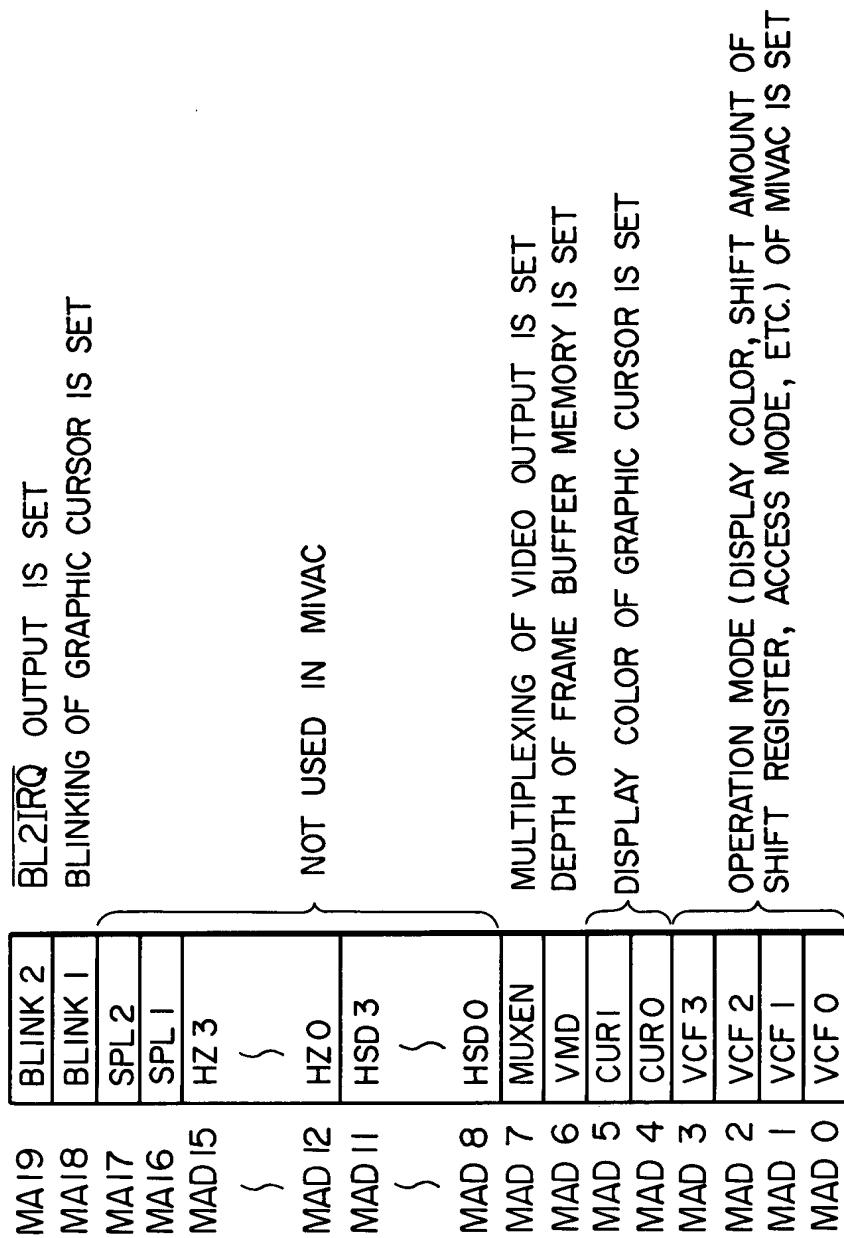


FIG. 11

CURSOR DISPLAY COLOR		
CUR I	CUR O	
0	0	BLACK (VIDEO A - VIDEO D = 0)
0	-	WHITE (VIDEO A - VIDEO D = 1)
-	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D
-	-	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO C (VIDEO D IS KEPT UNCHANGED)

## FIG. 8



## FIG. 9

MODE	CRT SCREEN LAYOUT EXAM- PLE (DOTS X RASTER)	MAXIMUM FRAME BUFFER CA- PACITY (BYTES)	ACRTC OP- ERATION FREQUENCY (MHz)	MEMORY ACCESS SPEED	HIGH- SPEED DRAWING	NUMBER OF MEMO- RIES	COLOR/ GRA- DATION	SHIFT AMOUNT (BITS)	MAXIMUM DOT CLOCK FREQ. (MHz)
0	640x200, 350, 400, 480	512K/128K				1	4	8	16.5
1	640x200, 480x240, 320x200, 240					—	16	4	8.25
2	320x200, 240					—	4	16	33
3	266x192					—	2	16	8
4	640x200, 350, 400, 480	IM/256K				4	16	8	16.5
5	640x200, 480x240, 320x200, 240	2M/512K				4	16	33	16.5
6	640x200, 480x240, 320x200, 240	512K/128K				—	16	8	16.5
7	320x200, 240					—	4	8	8.25
8	256x192					—	32	33	33
9	640x200, 350, 400, 480	IM/256K				○	2	4	16
A	640x200, 350, 400, 480	2M/512K				—	16	8	8.25
B	640x200, 350, 400, 480					4	16	16	16.5
C	640x200, 480x240, 320x200, 240					4	16	16	16.5
D	640x200, 350, 400, 480	512K/128K				—	4	32	33
E	640x200, 480x240, 320x200, 240	IM/256K				960ns/ 16ACCESSES	—	16	16.5
F	640x200, 350, 400, 480					2	32	33	33

4.13

F I G. 10

MODE	DOT CLOCK FREQUENCY
O, 3, 5, 8 B, D, F	33MHz ~ 11MHz
I, 4, 6, 9 C, E	16.5MHz ~ 5.5MHz
2, 7, A	8.25MHz ~ 2.75MHz

F I G. 12

VMD	MEMORY CHIP EMPLOYED
O	256 K × 4BIT DRAM
I	1M × 4BIT DRAM

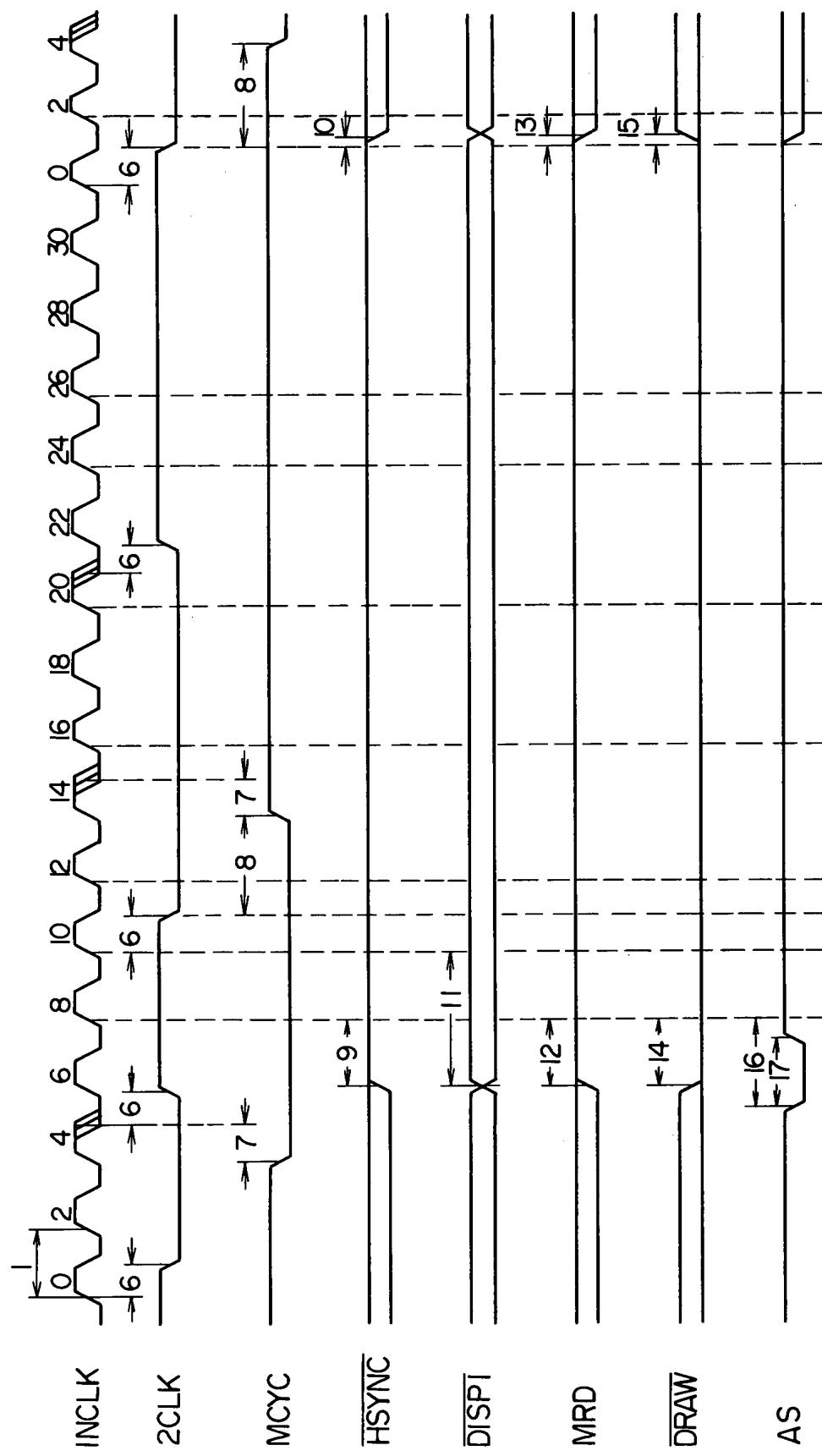
F I G. 13

MUXEN	VSYNC / 2	VIDEO A	VIDEO B
O	O	A	B
	I	A	B
I	O	A	B
	I	C	D

F I G. 14

BLINK I	GRAPHIC CURSOR DISPLAY
O	NOT DISPLAYED
I	DISPLAYED

FIG. 15a



F | G. | 5b

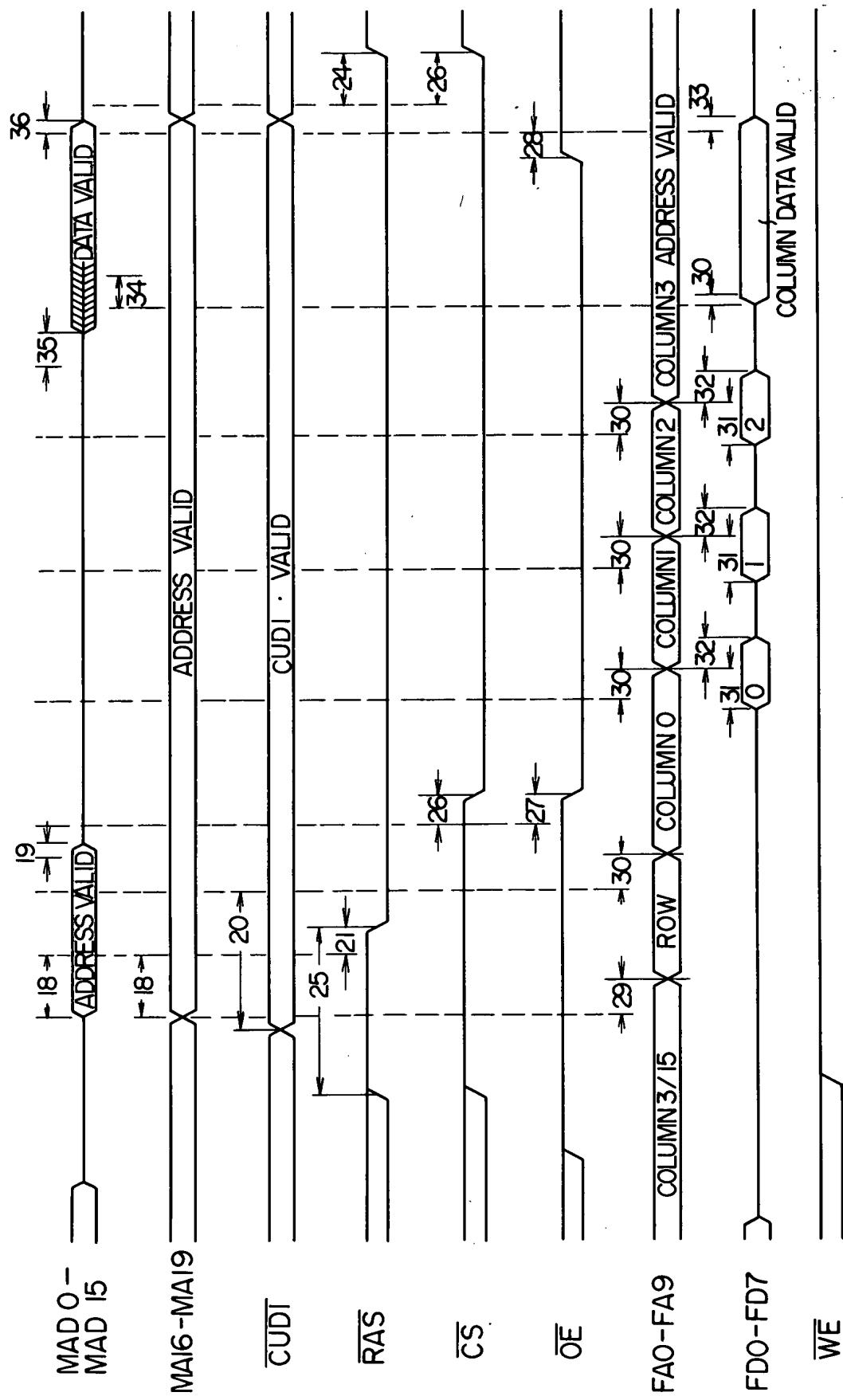


FIG. 16a

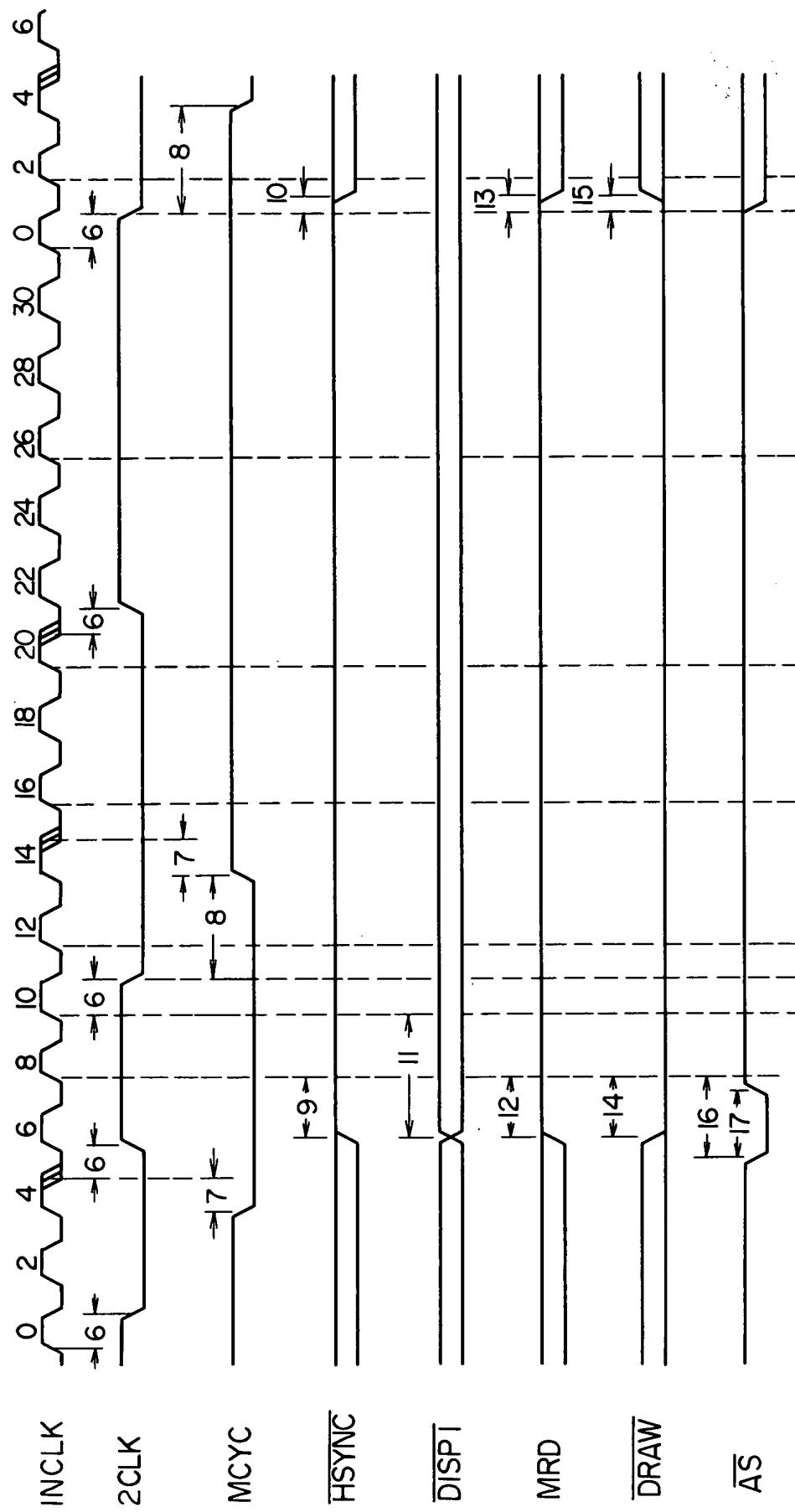


FIG. 16b

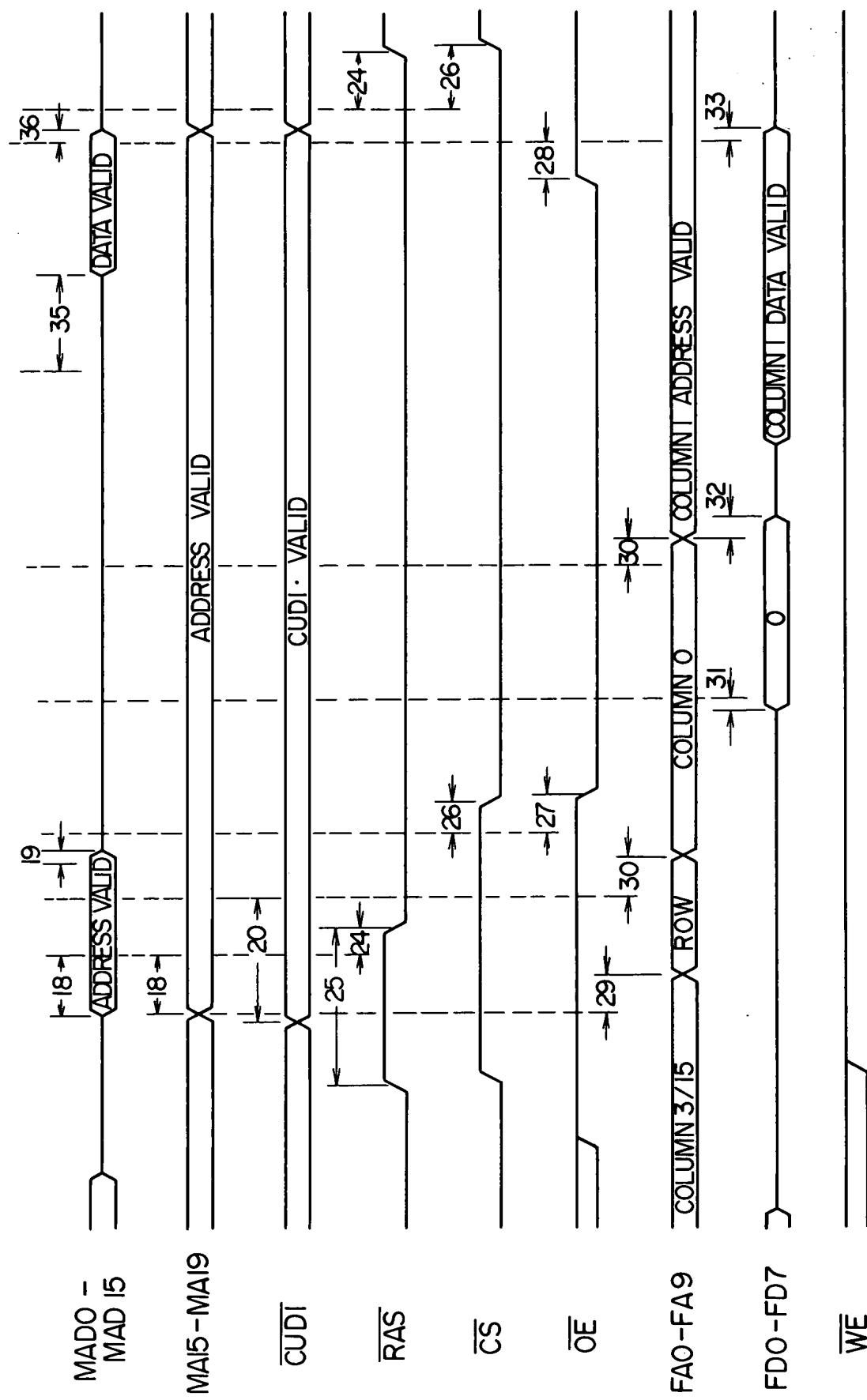
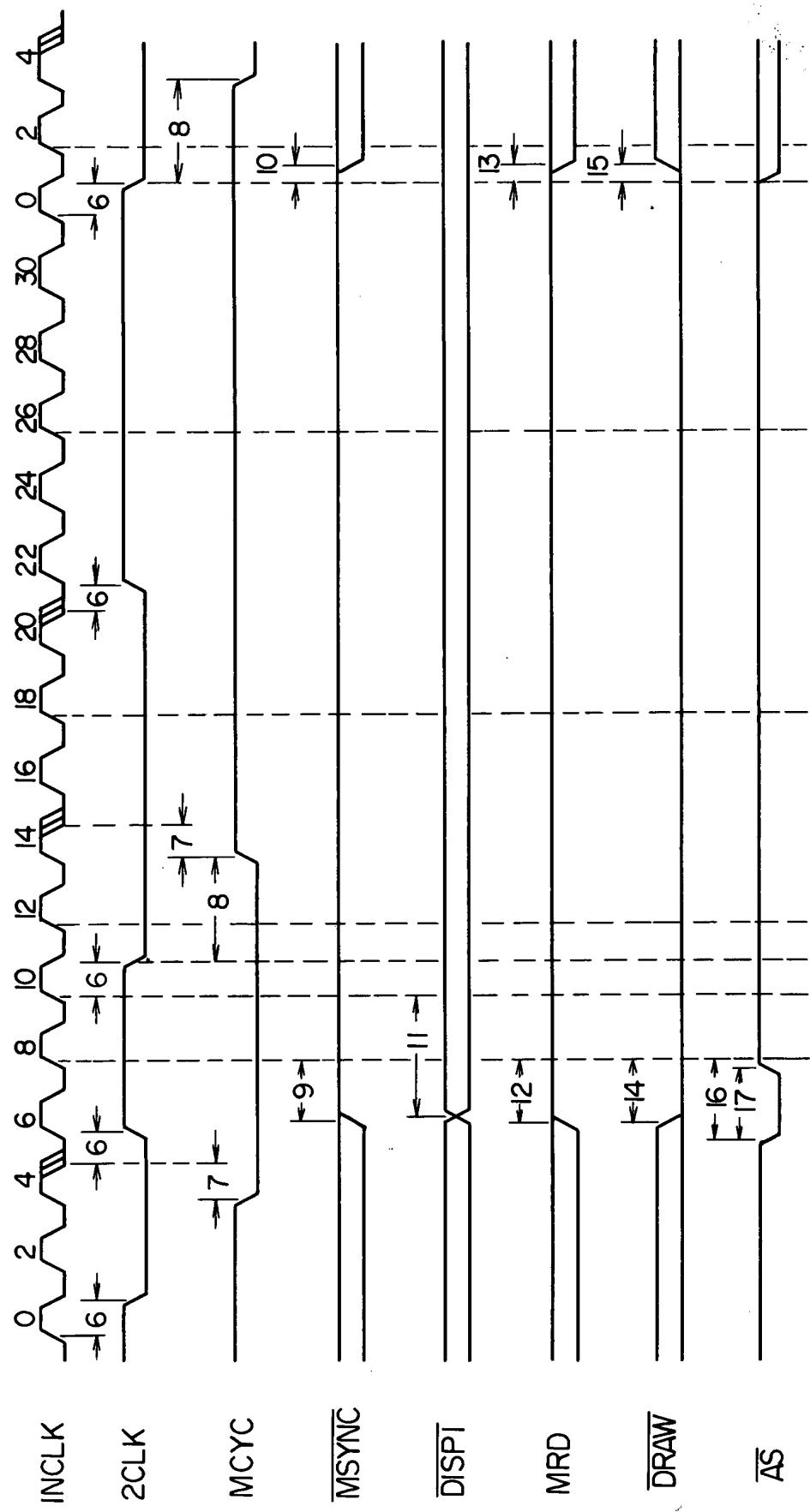


FIG. 17a



F I G. 17b

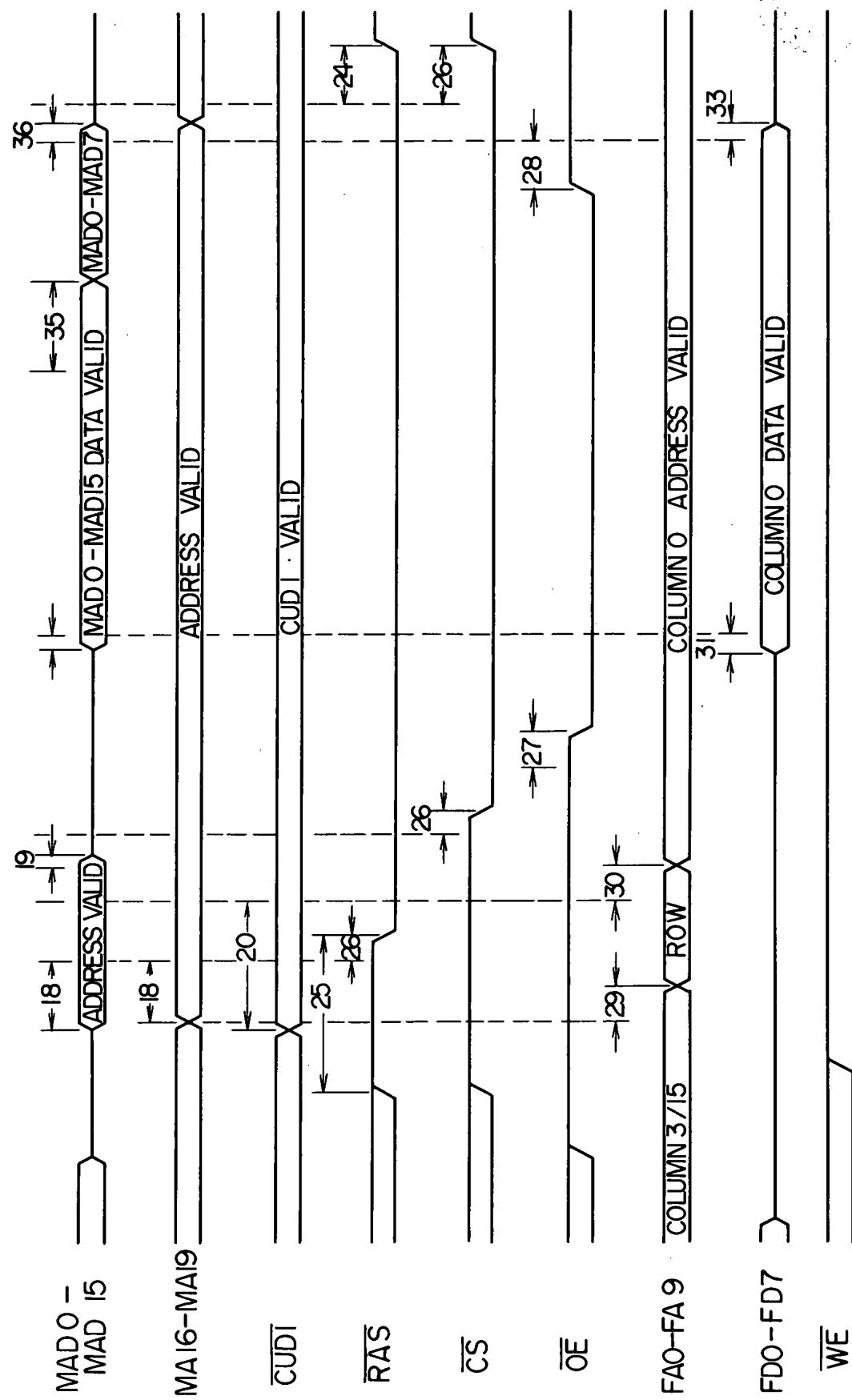


FIG. 18a

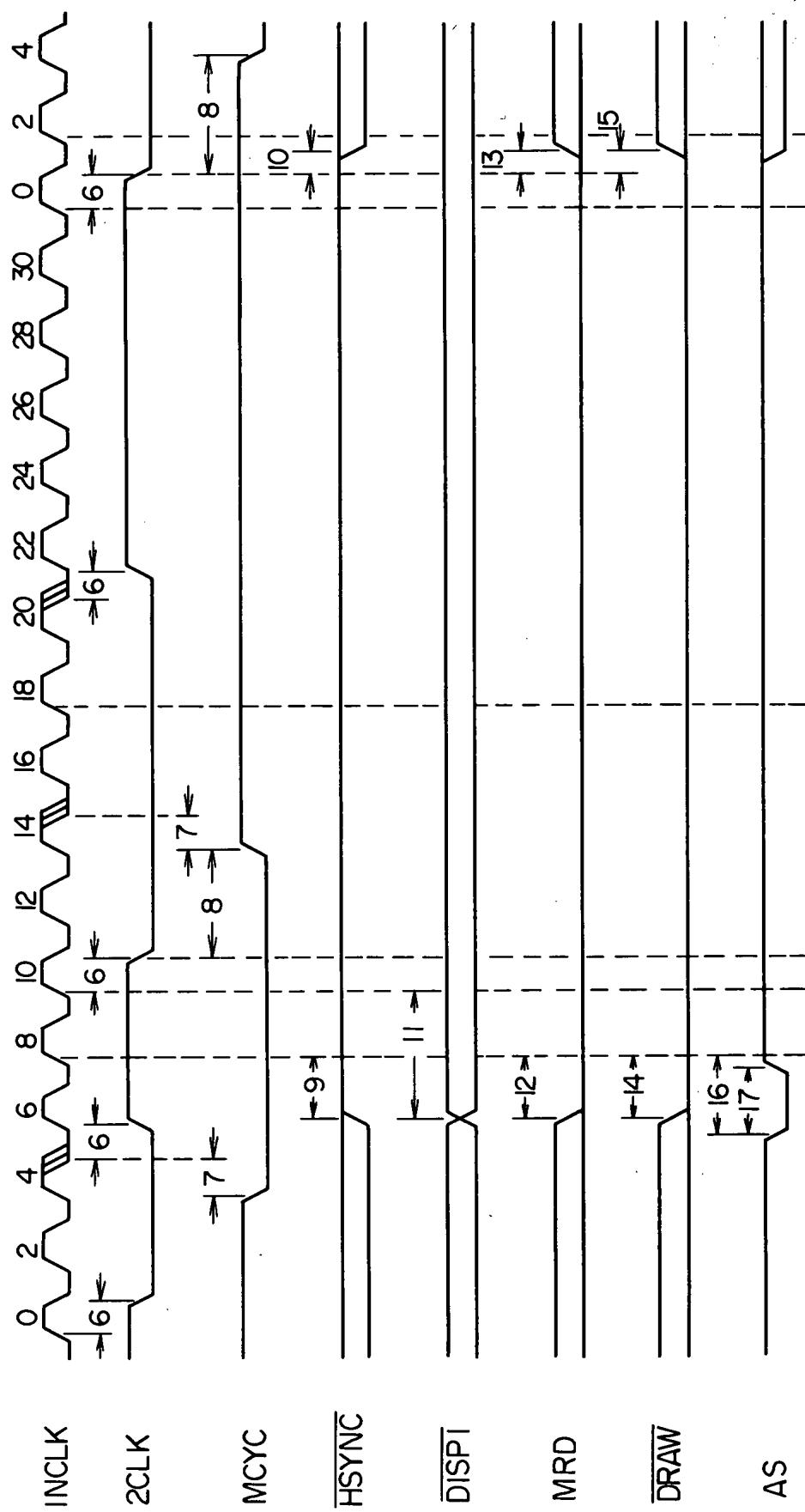


FIG. 18b

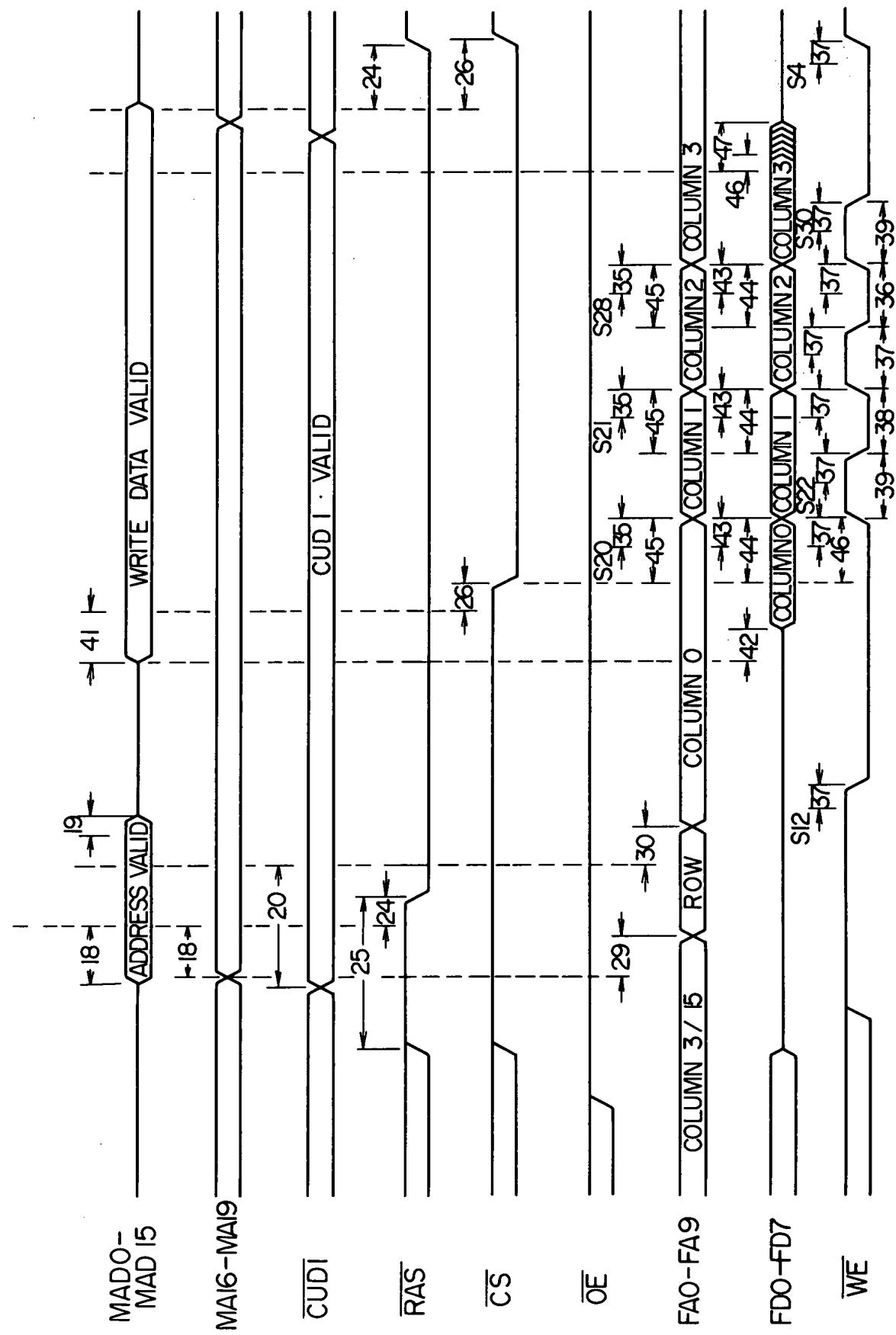


FIG. 19a

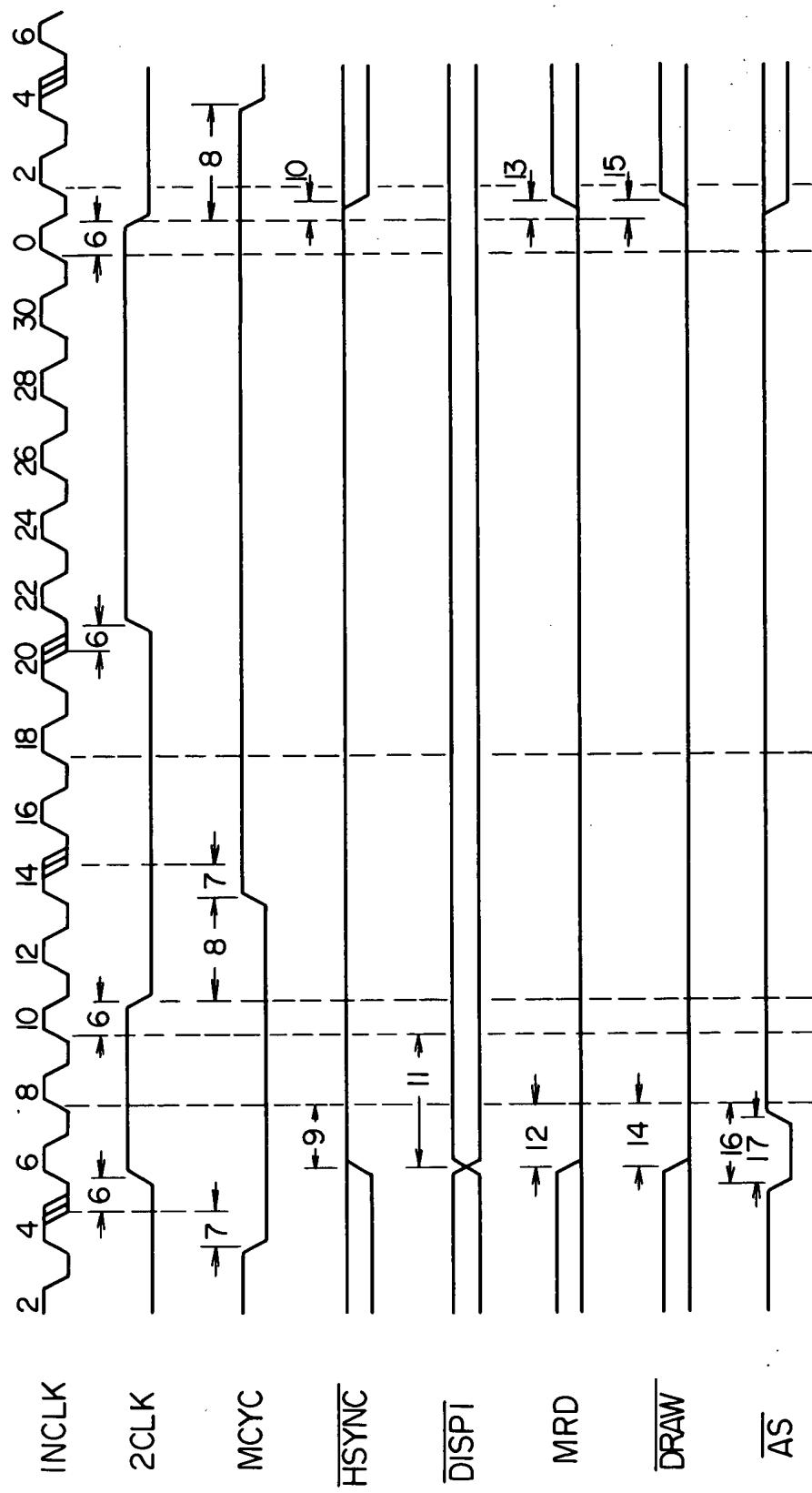


FIG. 19b

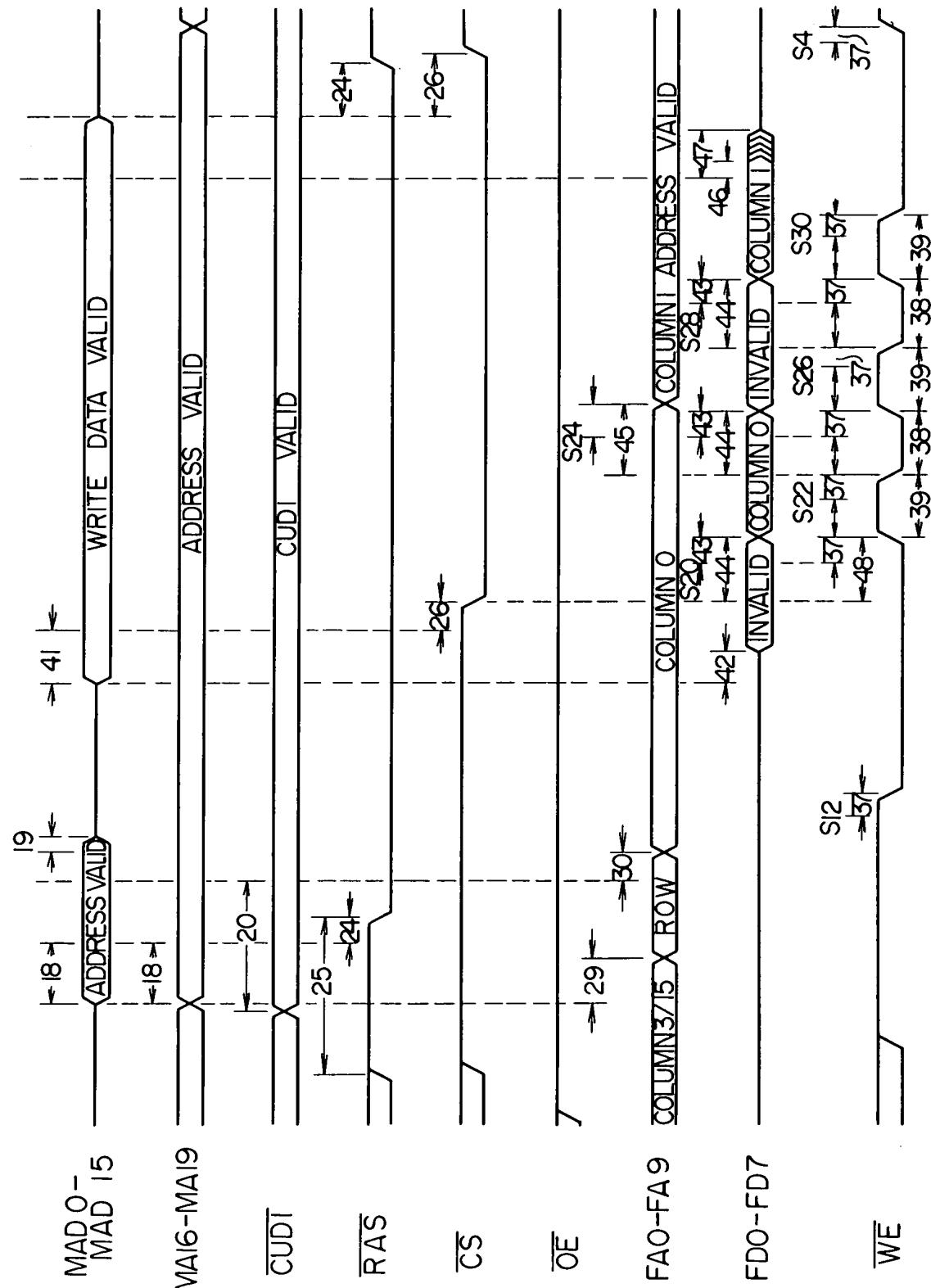


FIG. 20a

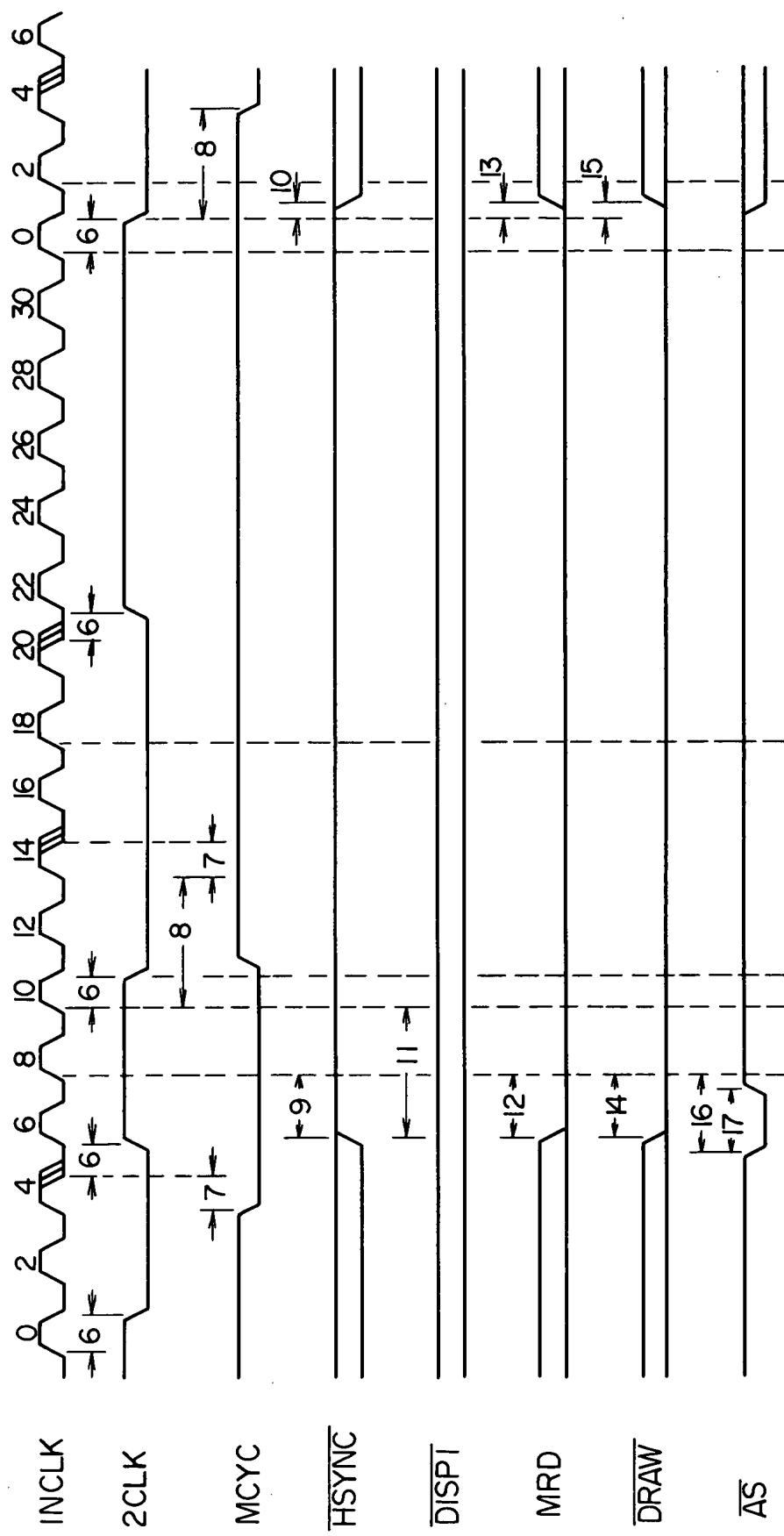


FIG. 20b

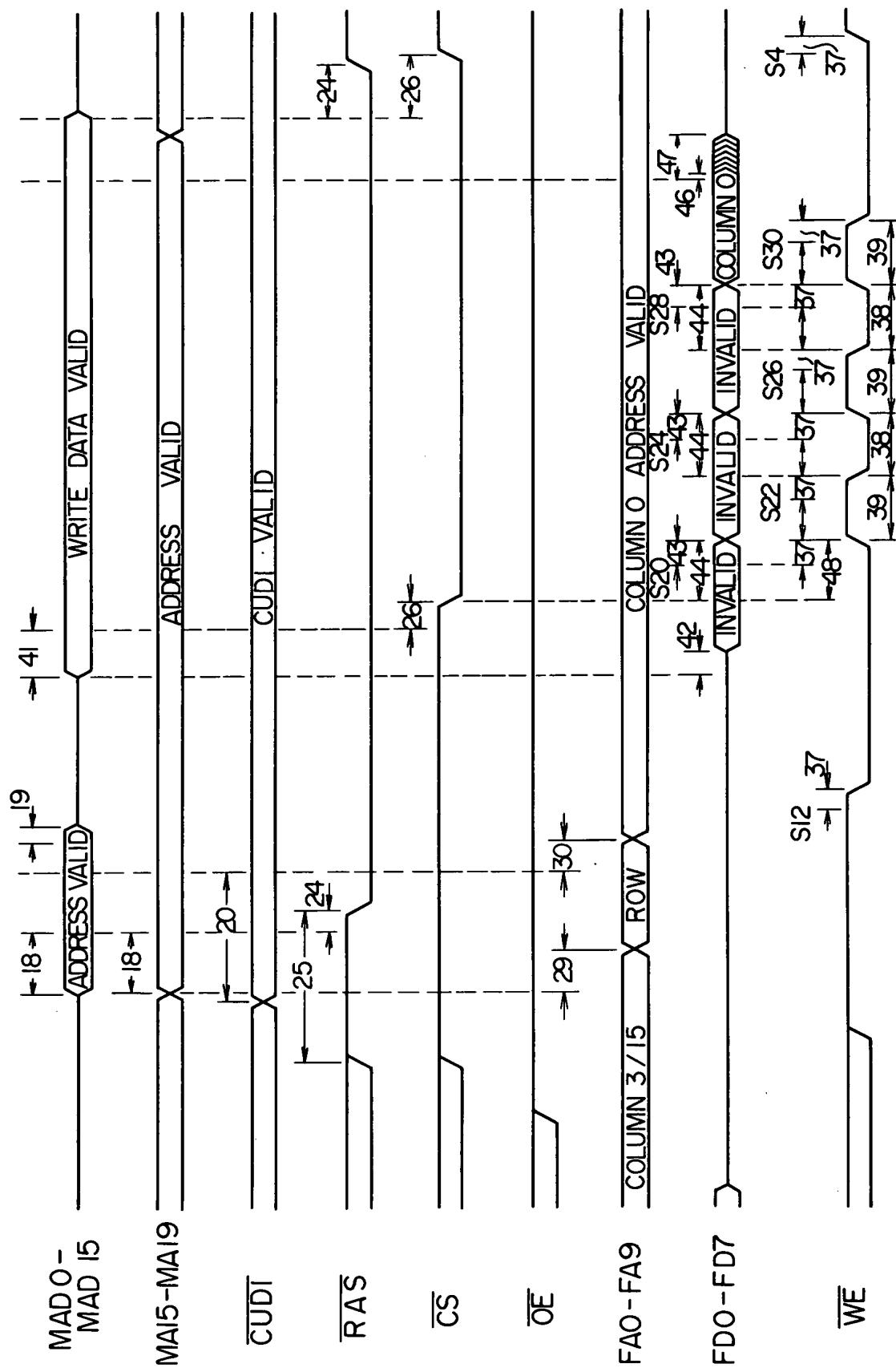


FIG. 21a

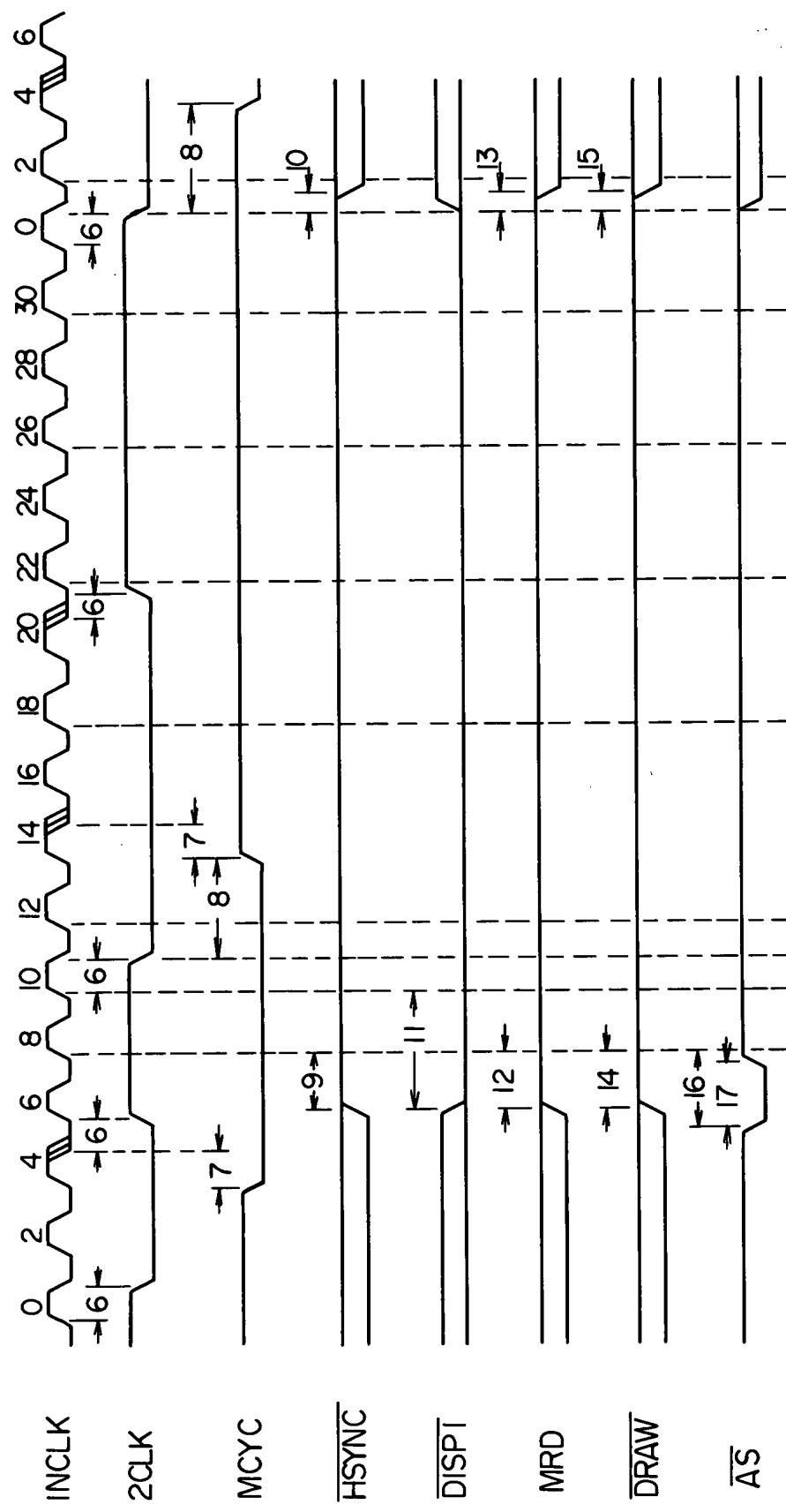
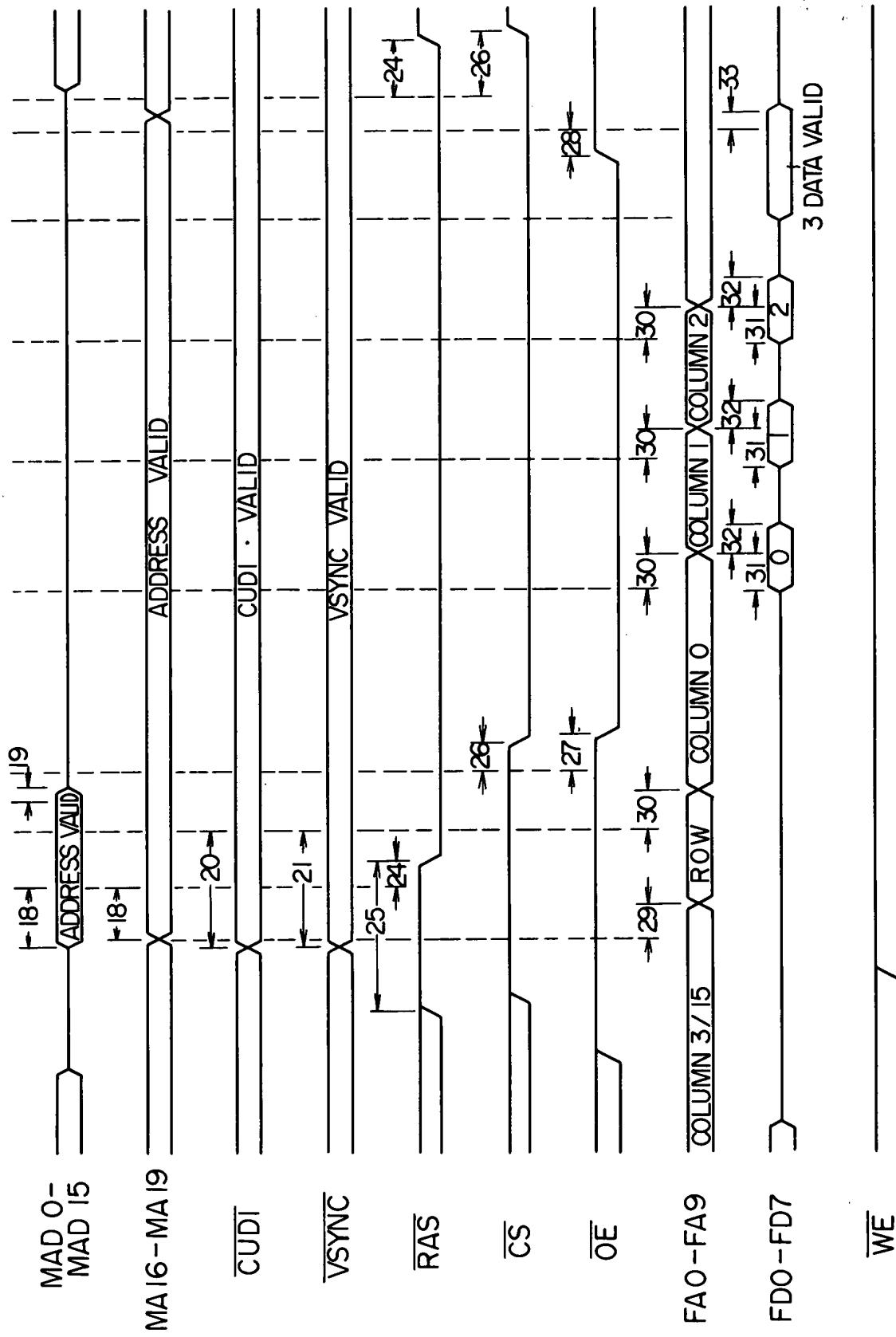
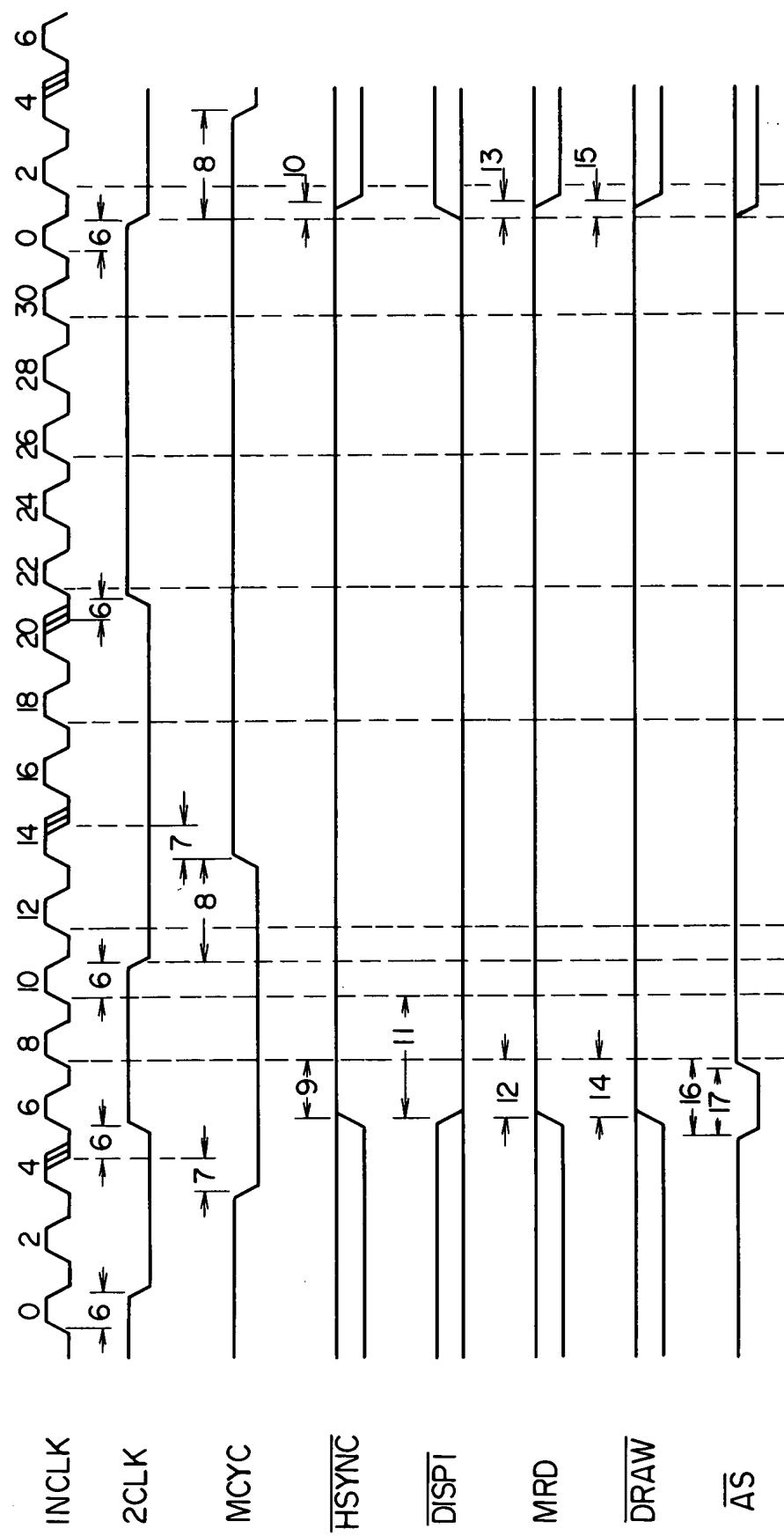


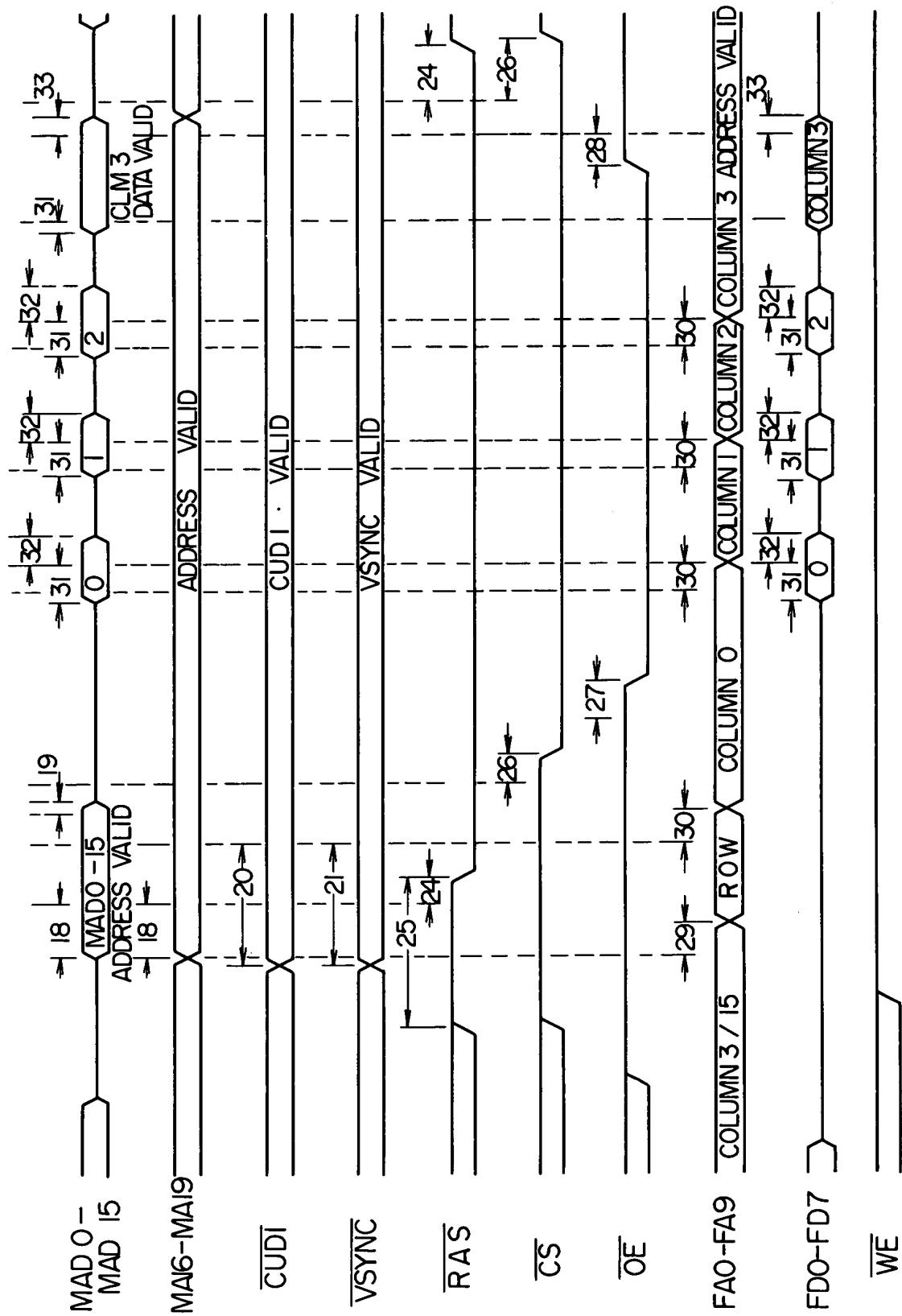
FIG. 21b



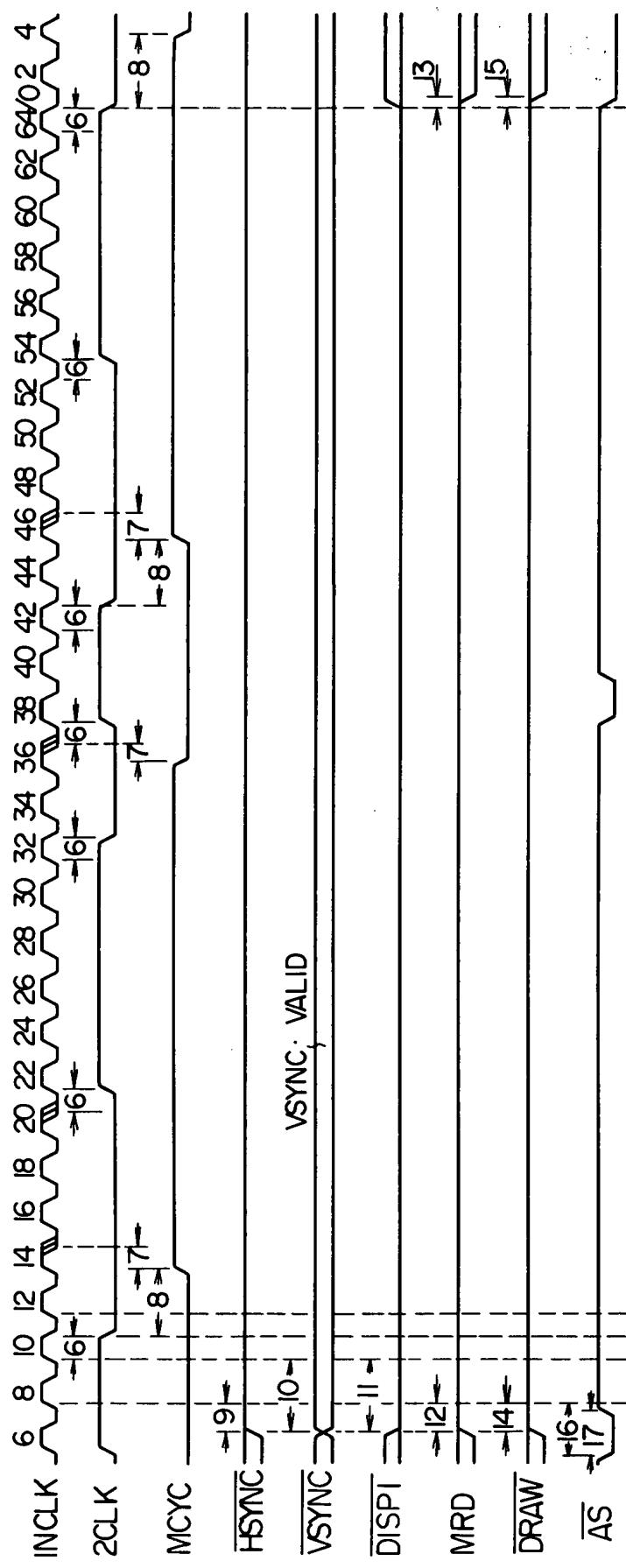
F 1 6. 22a



F I G. 22b



F I G. 23a



F - G. 23b

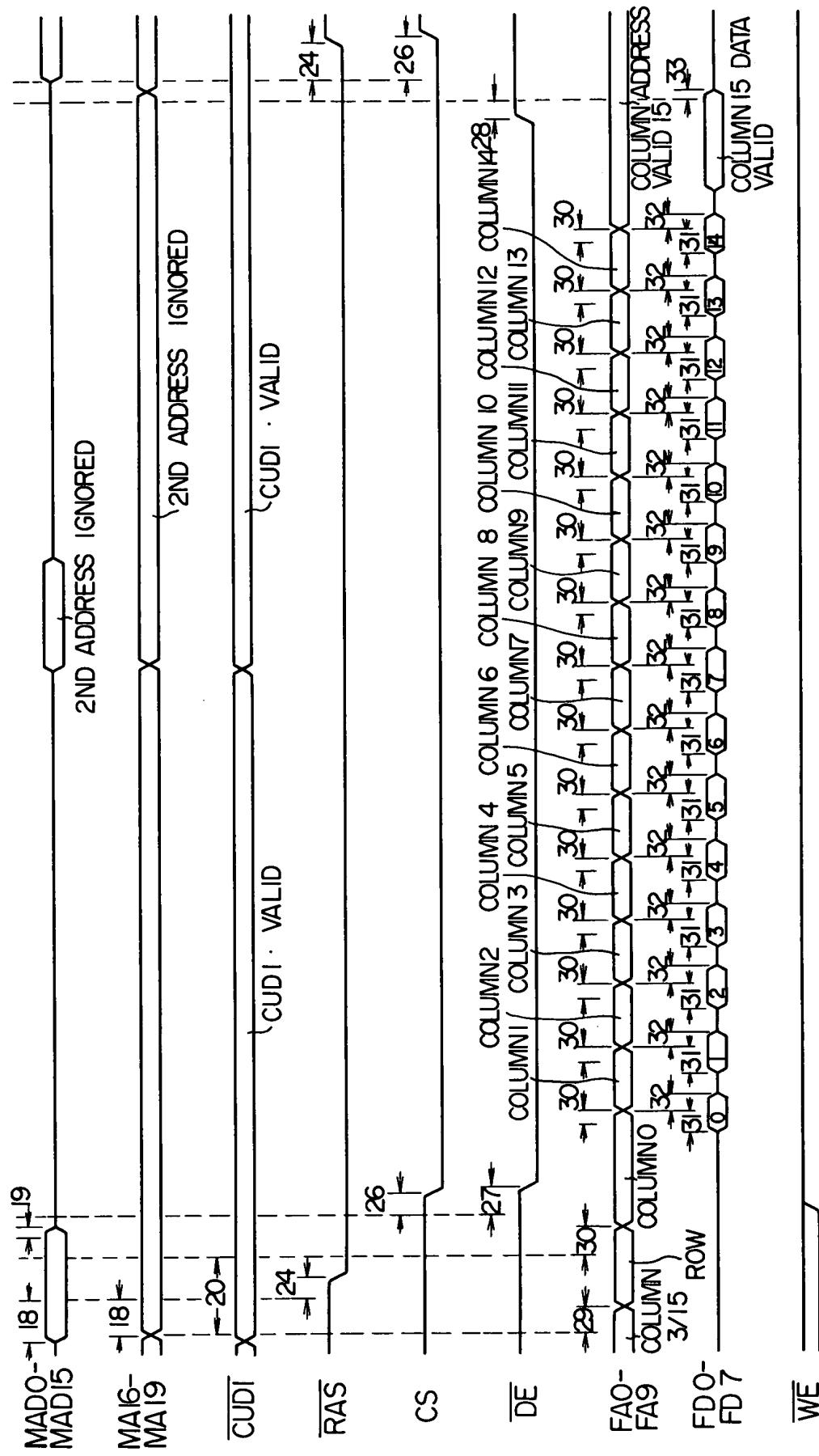


FIG. 24a

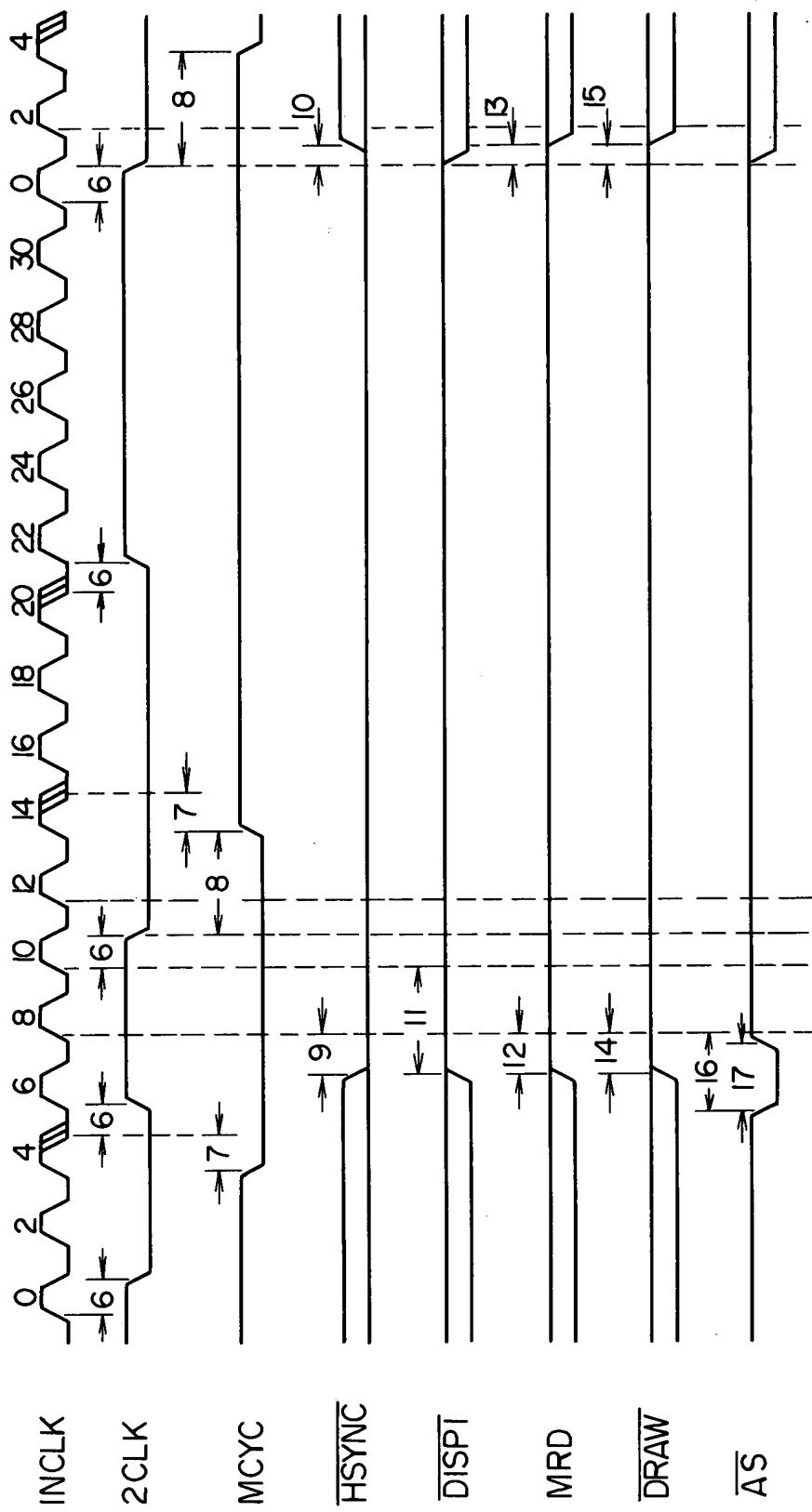
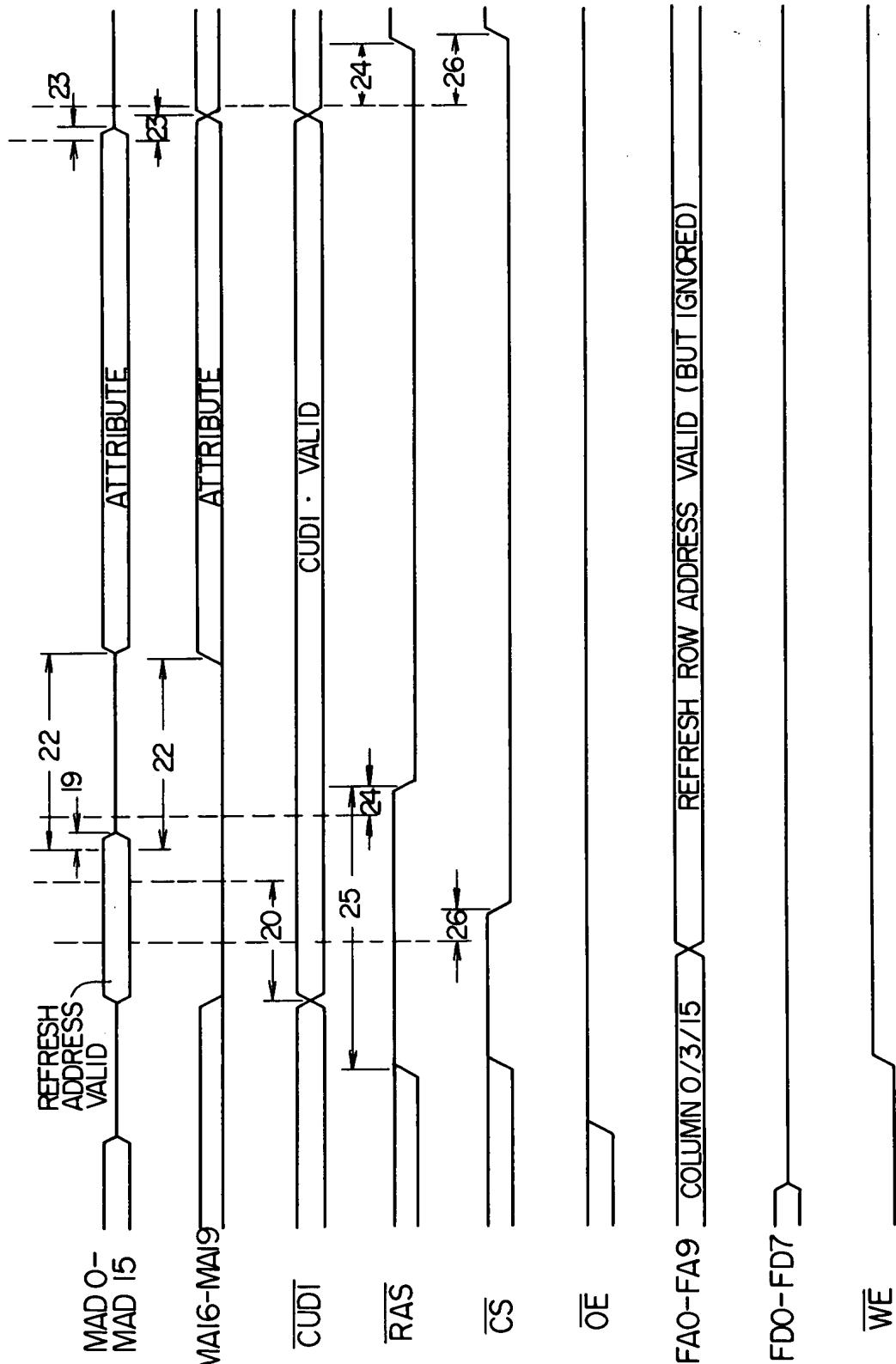
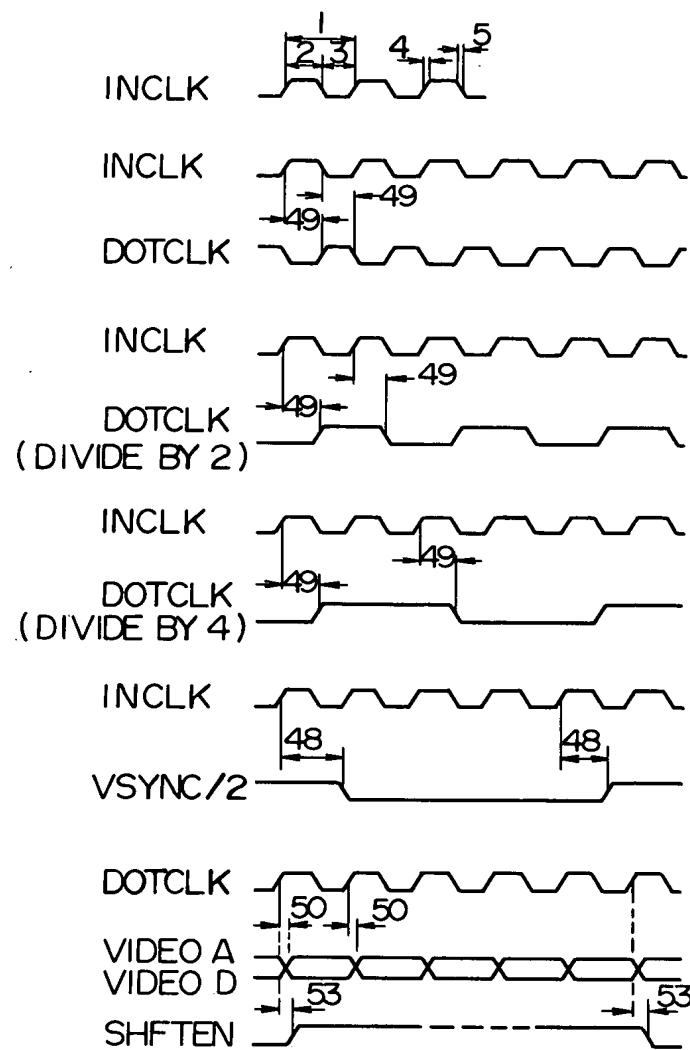


FIG. 24b



F I G. 25



F I G. 26

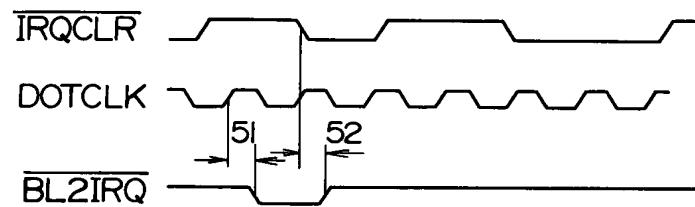
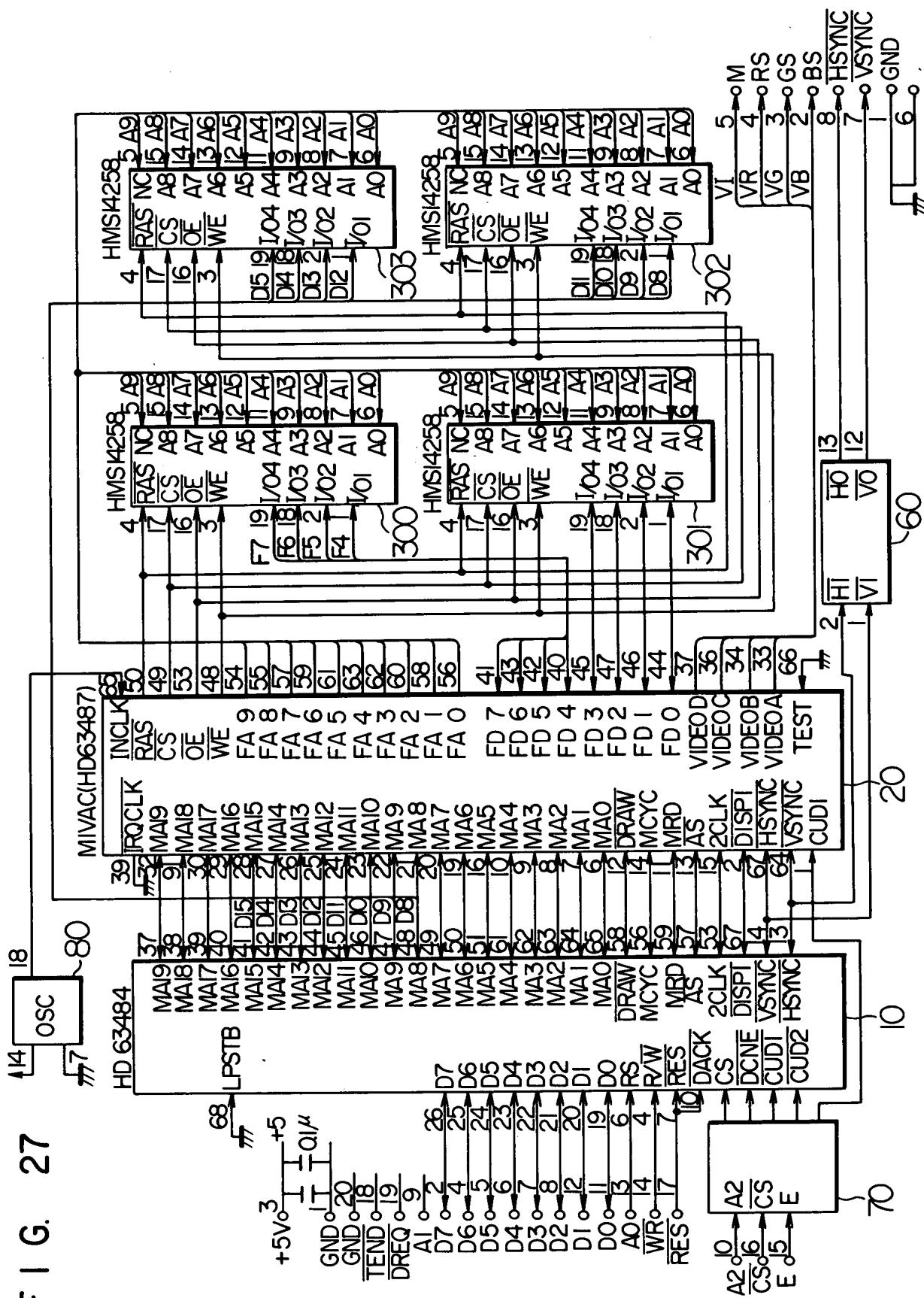
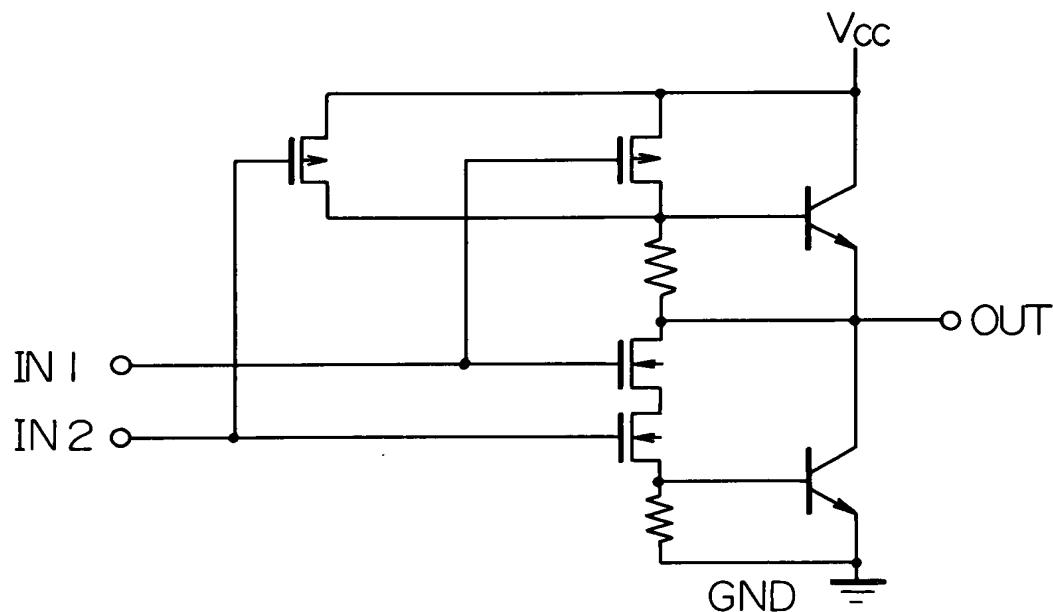


FIG. 27



F I G. 28



F I G. 29a

FA	4 ACCESSES / MCYC (DRAW, DISPLAY)				16 ACCESSES / 2 MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MAD 8	<u>NCO</u>	-	-	MAD 8	<u>NCO</u>
8	MAD 9	<u>NC 1</u>	MAD 9	<u>NC 1</u>	MAD 9	<u>NC 1</u>	MAD 9	<u>NC 1</u>
7	MAD 8	<u>NC 2</u>	MA 17	MAD 7	MAD 8	<u>NC 2</u>	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	<u>WCT</u>	MAD 11	<u>WCT</u>
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	<u>WC 0</u>	MAD 10	<u>WC 0</u>

□ : COLUMN ADDRESS COUNTER

F I G. 29b

2 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)				16 ACCESSES / 2MCYCS (DISPLAY)				
FA	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	<u>NC0</u>	-	-	MA 18	<u>NC0</u>	-	-	MA 18	<u>NC0</u>
8	MAD 9	<u>NC1</u>	MAD 9	<u>NC1</u>	MAD 9	<u>NC1</u>	MAD 9	<u>NC1</u>	MAD 9	<u>NC1</u>	MAD 9	<u>NC1</u>
7	MAD 8	MAD 7	MA 17	MAD 7	MA 8	MAD 7	MA 17	MAD 7	MA 8	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 5	MAD 5	MAD 15	MAD 5	MAD 5	MAD 5	MAD 5	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 4	MAD 4	MAD 14	MAD 4	MAD 4	MAD 4	MAD 4	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 3	MAD 3	MAD 13	MAD 3	MAD 3	MAD 3	MAD 3	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 2	MAD 2	MAD 12	MAD 2	MAD 2	MAD 2	MAD 2	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC 1	MAD 11	WC 1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	<u>WC0</u>	MAD 10	<u>WC0</u>	MAD 10	<u>WC0</u>	MAD 10	<u>WC0</u>

[ ] : COLUMN ADDRESS COUNTER

## F I G. 29c

FA	1 ACCESSES / MCYC ( DRAW )				4 ACCESSES / MCYC ( DISPLAY )			
	256K x 4 -BIT ( VMDO = 0 )		1M x 4 -BIT ( VMDO = 1 )		256K x 4 -BIT ( VMDO = 0 )		1M x 4 -BIT ( VMDO = 1 )	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	MAD 9	-	-	MA 18	MAD 9
8	MAD 9	MAD 8	MA 19	MAD 8	MAD 9	MAD 8	MA 19	MAD 8
7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WCO	MAD 10	WCO

[ ] : COLUMN ADDRESS COUNTER